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System Modeling of CMOS Power Amplifier Employing Envelope and Average Power Tracking for Efficiency Enhancement

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System Modeling of CMOS Power Amplifier Employing Envelope and Average Power Tracking for Efficiency Enhancement

by

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To My Family

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System Modeling of CMOS Power Amplifier Employing Envelope and Average Power Tracking for Efficiency Enhancement

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The University of Texas at Austin, 2012

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In the past decade, there has been great motivation to improve the efficiency of power amplifiers (PAs) in handset transmitter systems in order to address critical issues such as poor battery life and excessive heat. Currently, the focus lies on high data rate applications such as wideband code division multiple access (WCDMA) and long term evolution (LTE) standards due to the stringent efficiency and linearity requirements on the PA.

This thesis describes a simulation-based study of techniques for enhancing the efficiency of a CMOS power amplifier for WCDMA and LTE applications. The primary goal is to study the concepts of envelope and average power tracking in simulation and to demonstrate the effectiveness of these supply modulation techniques on a CMOS PA design.

The P1dB and IMD performance of a Class A/AB CMOS PA has been optimized to operate with high peak-to-average modulation with WCDMA

and LTE signals. Behavioral models of envelope and average power tracking are implemented using proposed algorithms, and a system-level analysis is performed.

Envelope tracking is seen to offer a peak PAE improvement of 15% for WCDMA, versus a fixed voltage supply, while average power tracking renders a maximum efficiency gain of 9.8%. Better than -33dBc adjacent channel leakage-power ratio (ACLR) at 5MHz offset and EVM below 4% are observed for both supply tracking techniques. For LTE, envelope and average power tracking contribute to a peak PAE enhancement of 15.3% and 7%, respectively. LTE ACLR begins failing the -30dBc specification above 22.5dBm output power during envelope tracking operation in the PA implementation described here.

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Introduction

1.1 Power Amplifier Efficiency Enhancement Techniques

1.1.1 Motivation

Modern handsets are required to support a high level of data transmission, mainly driven by new applications, such as mobile web browsing and video streaming. The handset transmitter system and specifically the power amplifier (PA) circuit are typically required to satisfy challenging efficiency and linearity requirements. A block diagram of a WCDMA handset transceiver is shown in Figure 1.1 [1].

Conventional PAs achieve peak efficiency near the maximum rated power for the device. At this power level however, PAs can also exhibit significant distortion. It is important to ensure sufficient linearity under such operating conditions. Another design aspect that needs to be considered is that as the drive power is reduced, in other words "backed-off," the efficiency is dramatically decreased and the average efficiency over a wide range of RF output levels is much lower than the peak efficiency [2]. This can lead to sub-optimal battery life and also cause the PA to generate excessive heat. These design constraints motivate the requirement for a solution that improves the

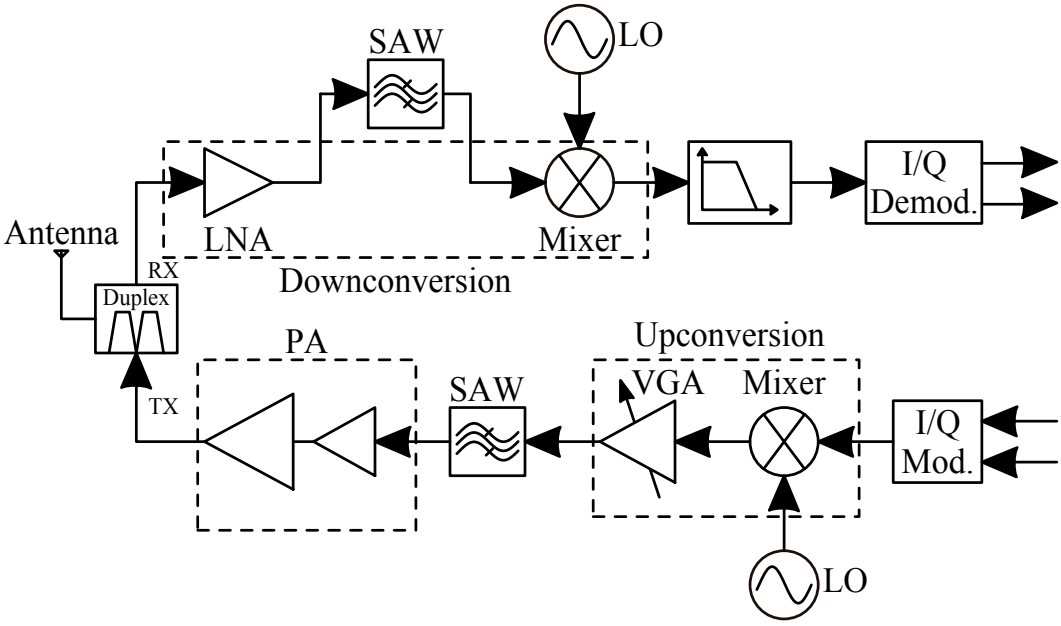

Figure 1.1: WCDMA handset transceiver.

average efficiency while ensuring that the linearity requirements are simultaneously met. Several efficiency enhancement techniques have been proposed to date. The next section will begin with an introduction to three classical approaches: the Doherty PA, the Envelope Elimination and Restoration (EER) technique, and the Linear amplification using Nonlinear Components (LINC) technique and will conclude with two alternative approaches: Envelope Tracking (ET) and Average Power Tracking (APT).

1.1.2 Doherty Technique

The Doherty PA was first proposed by William Doherty in 1936 to address the efficiency drop off at lower power levels [3]. This approach involved

what is also referred to as "active load-pull" concept [2], where the impedance of an RF load seen by one transistor (or vacuum tube) can be modified by applying a current from a second device. A simplified block diagram of a two-stage Doherty system which consists of two PAs in parallel and two quarter-wave transmission lines is shown in Figure 1.2 [4]. The drive control block functions as the biasing network with the main PA typically biased in Class AB while the auxiliary PA is biased in Class C.

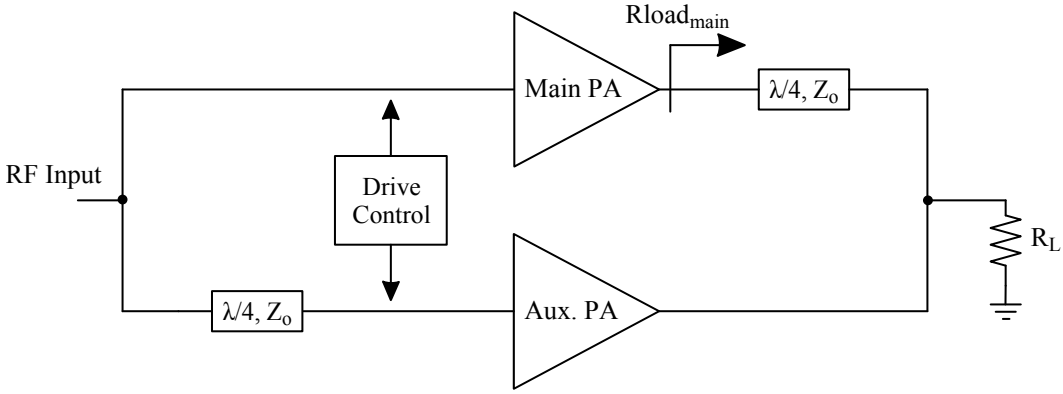

Figure 1.2: Doherty system block diagram.

At low output power levels, the auxiliary PA is turned off while the main PA is operating linearly. In this mode, the main PA sees an impedance of $Rload_{main}$, looking into the T-Line. Equation 1.1 relates the power $Pout$ that is delivered to the load and the amplitude V_{env}. If $Rload_{main}$ is increased as $Pout$ decreases, then the output envelope remains at a larger amplitude, which is effective in improving the efficiency at lower values of $Pout$.

$$Rload_{main} = \frac{V_{env}^2}{2 * Pout} \tag{1.1}$$

As the input voltage drive is increased, the main amplifier becomes saturated at a power level much less than the peak output power, for example, at half the maximum power. Thus, maximum efficiency is achieved well below the system peak-output power (PEP). The input level at which the main amplifier saturates is considered the transition point which in classical Doherty systems is located at half the maximum output voltage, $\frac{V_{DD}}{2}$ or approximately 6dB backoff. Once the main amplifier saturates, the auxiliary device turns on and operates as a controlled current source while the main amplifier starts to act as a voltage source. The quarter-wave transformer between the load resistor and the main device performs impedance inversion. The main device observes decreasing resistive impedance as the auxiliary device current increases. Since the combined RF output power of the two devices increases and the resistive load seen by the main amplifier decreases, the output voltage of the main amplifier remains constant. In this medium-power region, the efficiency of the main amplifier remains at its maximum value while the efficiency of the auxiliary amplifier begins to increase from the transition point and reaches its maximum value at PEP.

Advantages of Doherty [4]:

- Potentially simpler approach compared to EER or ET discussed below in that it does not require high-performance envelope modulators
- Not restricted by the modulator bandwidth such as in EER or ET

- Efficiency is equivalent to or better than EER, ET and outphasing methods

Disadvantages & limitations of Doherty [5]:

- Bandwidth limitation due to the use of the quarter-wave transmission line
- Gain degradation caused by the peaking amplifier (auxiliary amplifier)
- Low biasing of the auxiliary amplifier can degrade IMD performance
- Vulnerable to nonlinear behavior and may require linearization such as predistortion or feed-forward methods

1.1.3 LINC Technique

Another classical efficiency enhancement technique, "LINC" (Linear amplification using Nonlinear Components), refers back to Chireix's "Outphasing" proposal in 1935 [6]. Similar to the Doherty system, two RF power amplifiers are used as depicted in Figure 1.3 [2]. However in this case, the PAs can be highly nonlinear and then combined to form a linear RF PA system. The second distinction from the Doherty technique is that in order to benefit from using switching PAs (e.g., Class F, D), two constant amplitude, phase modulated input signals are provided to the PAs. With the use of a phase modulator at the input, the amplitude modulation information is encoded as a differential phase shift, amplified by the nonlinear devices and the original

AM is then recovered in a summing operation [2]. The separation of the amplitude and phase-modulated signal, $S_{in}(t)$, into two phase-modulated signals, $S_1(t)$ and $S_2(t)$, with constant amplitude is shown in Equations 1.2 - 1.6 [2].

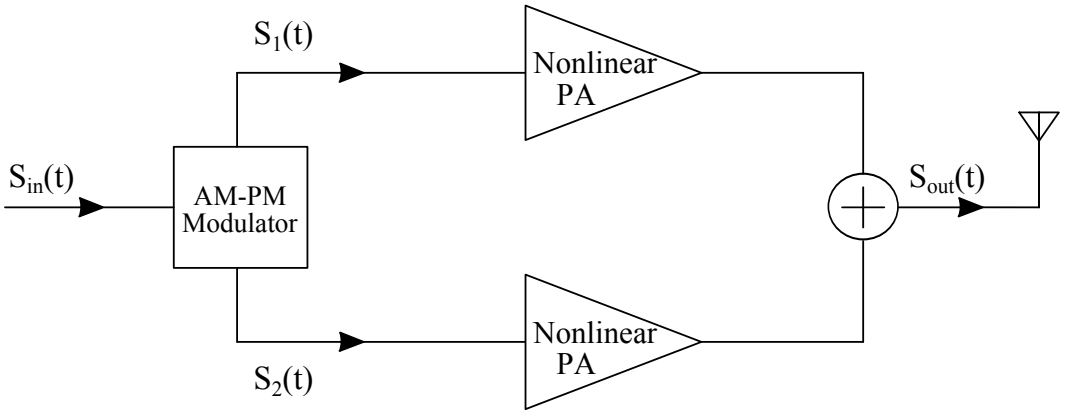

Figure 1.3: LINC system block diagram.

$$S_{in}(t) = A(t) \cdot cos(\omega t) \tag{1.2}$$

$$S_1(t) = cos[\omega t + cos^{-1}(A(t))] \tag{1.3}$$

$$S_2(t) = cos[\omega t - cos^{-1}(A(t))] \tag{1.4}$$

$$where\ \phi = cos^{-1}(A(t)) \tag{1.5}$$

$$S_{out}(t) = G \cdot (S_1(t) + S_2(t)) = 2 \cdot G \cdot A(t) \cdot cos(wt) \tag{1.6}$$

Since the overall efficiency scales with envelope amplitude, Chireix proposed that the outphasing power combiner be modified such that load modulation can take place between the two PAs. This would then maintain efficiency over a wide range of output power levels.

If the two nonlinear power devices in the outphasing amplifier are modeled as voltage generators connected differentially to a common load resistance, the impedance seen by each voltage generator consists of a resistive component equal to half the load resistance with a series reactance element that is dependent on the phase of the input signals. When the input signals are in-phase, $\phi = 90°$, they produce a peak envelope output. As ϕ decreases towards zero, the input signals become increasingly out of phase, the output envelope is reduced and the reactance component has a bigger impact on the RF load. Consequently, the efficiency is reduced. Chireix proposed inductive compensation to cancel out any capacitive reactance at the output of one of the amplifiers and capacitive compensation to cancel out inductive reactance for the other amplifier. In addition to the use of the high-efficiency PAs, design of such a combiner is critical to achieving efficiency enhancement in LINC.

Advantages of LINC:

- The distortion through a LINC system depends more on the AM to PM conversion process in the modulator than from the gain compression of the PAs themselves since they are driven by constant RF signal amplitudes. Therefore, the LINC system can be seen as a form of linearization,

assuming that the combiner does not introduce significant nonlinearities.

Disadvantages of LINC:

- Bandwidth and matching issues similar to Doherty
- Complexity in DSP is required to generate the drive signals, implement the AM to PM conversion and correct/calibrate gain and phase imbalances [1]

1.1.4 EER Technique

Envelope elimination and restoration (EER) was first proposed by Kahn in 1952 as an alternative efficiency enhancement approach to using a linear Class AB power amplification for single sideband (SSB) transmitters [7]. The general principle is to "eliminate" the RF envelope by passing it through a limiter and driving a highly efficient switching-mode power amplifier (Class D or E) with a constant amplitude phase-modulated carrier signal [2]. Then, with the use of an envelope detector and high level voltage supply modulator, the envelope amplitude can be "restored" at the supply node of the switching PA. The modulator can consist of a linear, high bandwidth amplifier (low efficiency) or a switching DC-DC converter (higher efficiency). The key block diagram components are shown in Figure 1.4 [8].

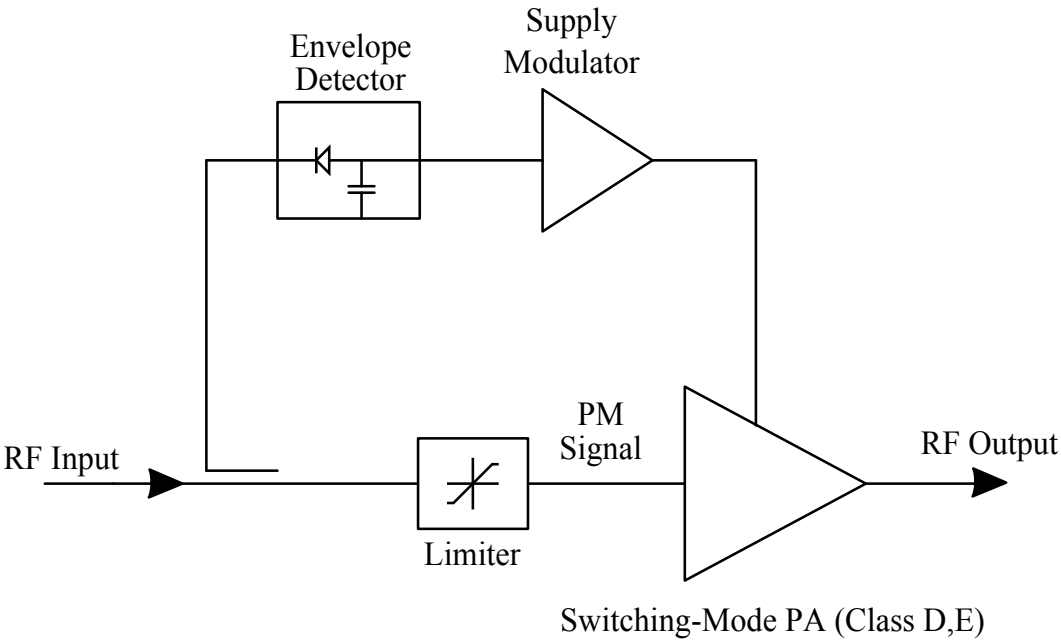

Figure 1.4: EER block diagram.

Theoretically, the EER process is much more efficient than a linear amplification approach because the switching-mode amplifier is always saturated and can remain efficient over supply voltage variation. However, the supply modulator will not operate with 100% efficiency and therefore, the efficiency of the overall system can be considerably degraded [2].

Advantages of EER:

- Theoretically can maintain high efficiency over a substantial range of envelope amplitude
- More flexibility in choosing the load impedance compared to fixed load impedance in Doherty and Chireix approaches

Disadvantages of EER [9]:

- Power consumption in both AM path (supply modulator) and PM path (limiter)
- In practice, the limiter is prone to variations in the phase modulation when the supply is varied. Furthermore, a hard-limited RF signal can also appear as intermodulation distortion (IMD) in the TX output.
- More sensitive to timing mismatch between RF and envelope amplitude paths than ET. Group delay of the two signal paths can introduce distortion.
- Constant-amplitude phase signal may require 10 times larger bandwidth than an I-Q modulation input signal due to the nonlinear transformation of I-Q to polar
- Envelope path may require 3-5 times larger bandwidth than the baseband I-Q input signal
- Cost and complexity due to DSP linearization overhead

1.1.5 Envelope Tracking

A variation to EER is the envelope-tracking (ET) system as shown in Figure 1.5 [8]. Both approaches provide an envelope amplitude-modulated signal to the supply of the PA. However, in ET, the entire envelope information (amplitude and phase) is amplified through a linear PA (Class A, B, AB).

Similar to EER, a high level voltage supply modulator is used to perform the tracking.

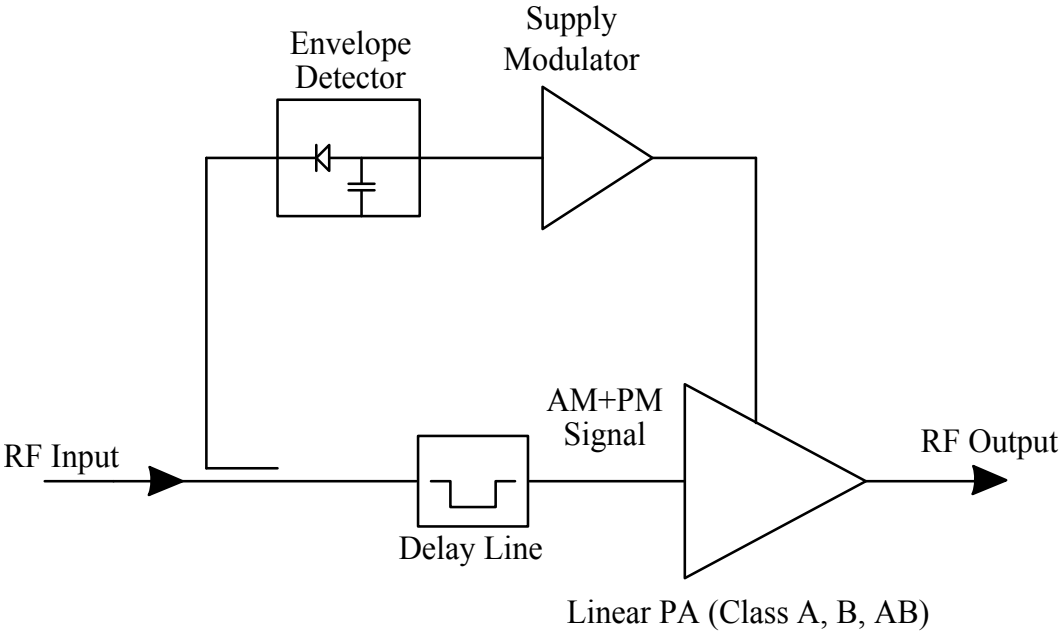

Figure 1.5: ET block diagram.

The main difference between ET/EER systems and Doherty/Chireix systems is that the load resistance is fixed in the former and the supply voltage is proportionally adjusted to the increasing input drive power. Thus, ET can better satisfy wider bandwidth applications because the efficiency enhancement operation can be completely decoupled from the output matching network. As the PA is backed off, the output envelope amplitude decreases and the supply can also be reduced to save DC power consumption. Therefore, maximum efficiency can be achieved over a wide linear power range. The ET implementation is easier than the EER architecture because the timing

mismatch between the RF and envelope paths is less of an issue. Compared to EER, the design of the modulator is relaxed since the envelope signal does not have to be "restored" and replicated with great accuracy [2]. This means that lower bandwidth tracking or solely tracking the peaks can still provide efficiency improvement and maintain signal fidelity.

The primary concern that arises in ET is from the efficiency loss in the supply modulator and noise contribution in the envelope amplitude path. For high bandwidth applications such as WCDMA and LTE, the limitations in the design of the modulator can become a bottleneck for the overall efficiency improvement. In addition, ET suffers from inherent gain variation/compression of the linear PA when the supply voltage and current are dynamically adjusted [10]. This can degrade linearity performance metrics such as adjacent channel leakage-power ratio (ACLR) and error vector magnitude (EVM), which will be discussed in Chapter 3. With respect to linearization, predistortion at baseband is also a popular solution although it adds cost and complexity to overall system.

1.1.6 Average Power Tracking

The average power tracking (APT) technique can be used as a slow-envelope tracking substitute for ET when a more efficient and lower bandwidth design for the supply modulator is preferred. The system is shown is Figure 1.6 [11]. Instead of instantaneously tracking both the slow and high frequency portions of the envelope, APT monitors the average power level and corre-

spondingly adjusts the voltage and/or current supplying the linear PA [11]. At low output power levels, the envelope amplitude becomes quite small and APT may render higher efficiency than ET.

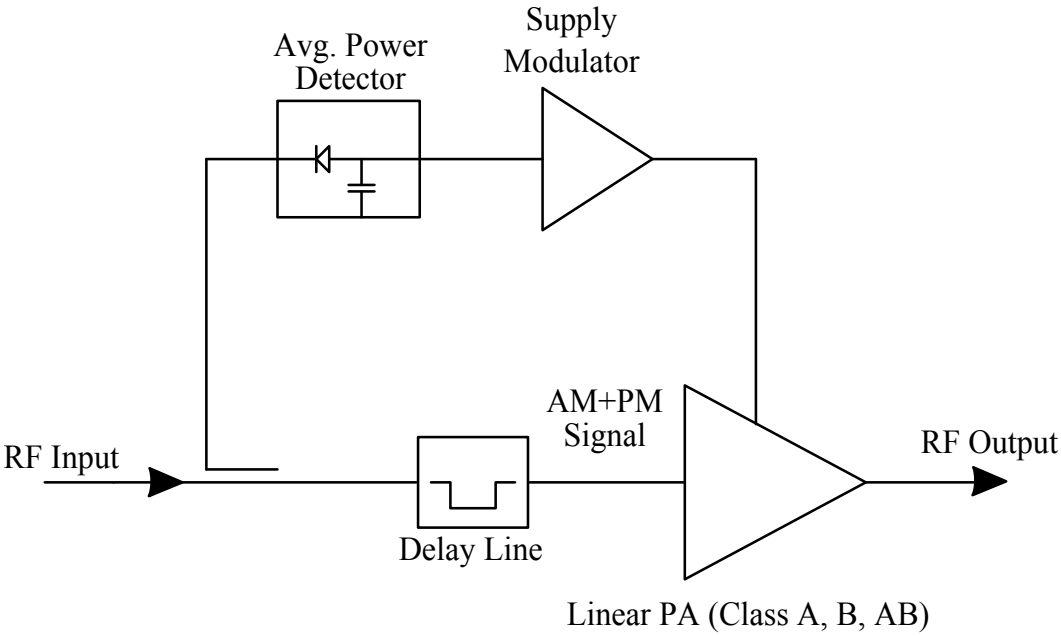

Figure 1.6: APT block diagram.

1.1.7 Efficiency Comparison

[12] describes the theoretical efficiency curves for the efficiency enhancement techniques that were previously discussed. This characterization assumes ideal power amplifiers that are driven by a continuous wave (CW) input. A conventional Class A power amplifier achieves the lowest efficiency since it is conducting at all times and constantly consuming power. The instantaneous efficiency is proportional to the output power and reaches 50% at PEP. A conventional Class B PA is conducting half of the time and therefore benefits

from a higher average efficiency curve and peak efficiency of 78.5%. Envelope tracking and Kahn's EER technique provide the best average efficiency over a wide range of output amplitude. Both of these curves assume zero loss supply modulators. In practice, the ET and EER efficiency curves will be further reduced at lower output amplitudes. The load-modulation based approaches, Chireix and Doherty, achieve as high of an efficiency as EER in the mid to high output amplitude levels but begin to significantly drop off at lower amplitudes.

1.2 Wireless Communication Standards

Since the advent 2G cellular systems, such as GSM (Global System for Mobile Communications) in 1991, the world has witnessed a rapid growth in the number of mobile handset devices. These 'second generation' (2G) phones that primarily utilized the GSM standard as a form of portable communication quickly transitioned into multimedia devices that could accommodate both "voice" and "data" services, such as access to internet browsing. This demand for wider bandwidth and data rates in the range of Mbit/s resulted in the development of 3G technology such as wideband code division multiple access (WCDMA) in 1999 [13].

Since then, the pace at which the next generation standards are evolving has only increased. The first pre-4G (3.9G) release of Long Term Evolution (LTE), Release 8 E-UTRA, has improved data throughput up to hundreds of Mbit/s. LTE Advanced, which is not to be confused with LTE, is considered LTE Release 10 and will become the first fully compliant 4G technology of the

future. Both will consist of the same core technology however LTE Advanced will have certain improvements such as even higher data rates over 1 Gbit/s [14, 15]. In this thesis, the original LTE Release 8 E-UTRA, will be studied. Sections 1.2.2 and 1.2.4 introduce some important technical specifications for WCDMA and LTE, respectively.

1.2.1 WCDMA

WCDMA [16, 17] supports data rates up to 2 Mbit/s (indoors) and 384 kbit/s (outdoors) through the use of a wide channel bandwidth of 5MHz. It employs a spread spectrum transmission in the form of code division multiple access (CDMA) which uses a spreading code to encode data that is to be transmitted for a given user. The data can then be decoded only by the desired recipient while all the other spreading codes occupied by other users appear as noise. This is what allows CDMA to utilize several users simultaneously in the same frequency band. A frequency division duplex (FDD) scheme is utilized for the uplink (mobile to base station) which means that the transmitter and receiver are operating at the same time however at different carrier frequencies. Due to this simultaneous operation, interference arising from the transmitter channels can corrupt the receiver channels. The data modulation scheme for uplink is in the form of binary phase shift keying (BPSK) which enables one bit of information to be transmitted for every symbol.

1.2.2 WCDMA Power Amplifier Requirements

The *3GPP TS 25.101* technical specification [18] document defines the RF characteristics and minimum performance requirements of the FDD mode of WCDMA for the User Equipment (UE). Table 1.1 shows some of the important WCDMA frequency and power requirements. Different power levels for each power class specify the maximum transmitted power at the antenna. For the purposes of this study, it will be assumed that there exists a 1-2 dB loss in the duplexer. For example, the maximum average output power at the PA will need to be in the range of 25-26 dBm for power class 3.

Table 1.1: 3GPP WCDMA FDD operating bands and power classes.

Operating Band	Uplink Frequency	Power Class 1	Power Class 2	Power Class 3	Power Class 4
I	1920 - 1980 MHz	33 dBm	27 dBm	24 dBm	21 dBm
II	1850 - 1910 MHz	-	-	24 dBm	21 dBm
III	1710 - 1785 MHz	-	-	24 dBm	21 dBm
IV	1710 - 1755 MHz	-	-	24 dBm	21 dBm
V	824 - 849 MHz	-	-	24 dBm	21 dBm
VI	830 - 840 MHz	-	-	24 dBm	21 dBm

1.2.3 LTE

A dramatic increase in data transmission rates is the major upgrade from WCDMA to pre-4G LTE [14]. Even though LTE Release 8 is considered as an evolution of the 3GPP 3G standards, it has incorporated an orthogonal frequency division multiple access (OFDMA) / single carrier frequency division multiple access (SC-FDMA) radio interface. OFDM (orthogonal frequency division multiplex) is used for downlink as a method of transmission that uses "orthogonal" sub-carrier signals, each modulated with a conventional modulation scheme such as quadrature amplitude modulation (QAM) or phase shift keying (PSK) at a low data rate. The sub-carriers' orthogonal behavior prevents mutual interference from occurring and a more accurate reconstruction of the signals as a result. The power amplifier efficiency is of more importance for LTE uplink because the majority of the power is consumed in the PA while the mobile device is transmitting to the base station. A smaller peak to average power ratio (PAPR) is desired to maximize PA efficiency and since OFDMA has a high PAPR, LTE uses a single carrier alternative, SC-FDMA. This hybrid format combines low PAPR while maintaining a high degree of resilience to multipath reflections and interference [19]. There are three modulation types that are supported in LTE: QPSK, 16QAM and 64QAM. Also a variety of channel bandwidths are offered namely, 1.4MHz, 3MHz, 5MHz, 10MHz, 15MHz and 20MHz. The higher order modulation formats and larger channel bandwidths will generate higher data rates, up to several hundred Mbit/s [20].

1.2.4 LTE Power Amplifier Requirements

The *ETSI TS 136 101* technical specification [20] document defines the RF characteristics and minimum performance requirements for evolved universal terrestrial radio access (E-UTRA) UE. Table 1.2 shows some of the important LTE frequency and power requirements. The frequency bands are common between WCDMA and LTE, however the maximum average output power for LTE is lower. The possible channel bandwidths for E-UTRA Band 1 are shown in Table 1.3.

Table 1.2: 3GPP LTE FDD E-UTRA operating bands and power classes.

E-UTRA Band	Uplink Frequency	Power Class 1	Power Class 2	Power Class 3	Power Class 4
1	1920 - 1980 MHz	-	-	23 dBm	-
2	1850 - 1910 MHz	-	-	23 dBm	-
3	1710 - 1785 MHz	-	-	23 dBm	-
4	1710 - 1755 MHz	-	-	23 dBm	-
5	824 - 849 MHz	-	-	23 dBm	-
6	830 - 840 MHz	-	-	23 dBm	-

Table 1.3: 3GPP LTE FDD E-UTRA channel bandwidth.

E-UTRA Band	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz
1	-	-	Yes	Yes	Yes	Yes

In this study, the PA is designed for a common Band I/1 (1950MHz carrier) and power class 3 (24dBm (WCDMA)/23dBm (LTE)). The other important specifications shown in Tables 1.4 and 1.5 are based off of compliance from [18] and [20], respectively. The main linearity performance metrics are defined by adjacent channel leakage-power ratio (ACLR) and error vector magnitude (EVM). These will be discussed in Chapter 3.

Table 1.4: WCDMA PA specifications.

Operating Frequency	1920 - 1980 MHz
Bandwidth	5 MHz
Maximum Output Power (@ Antenna)	24 dBm
$ACLR_{5MHz}$ (3.84 MHz integration bandwidth)	-33 dBc
$ACLR_{10MHz}$ (3.84 MHz integration bandwidth)	-43 dBc
EVM	4% (desired)

Table 1.5: E-UTRA (LTE) PA specifications.

Operating Frequency	1920 - 1980 MHz
Bandwidth	5,10,15,20 MHz
Maximum Output Power (@ Antenna)	23 dBm
$UTRA\ ACLR_1$, $UTRA\ ACLR_2$	-33 dBc / -36 dBc
$E-UTRA\ ACLR_1$	-30 dBc

1.3 Thesis Objective

This thesis will be focused primarily on the efficiency enhancement of a CMOS power amplifier for wireless handset applications using either WCDMA or LTE uplink. Due to the continuous advancement of PA supply modulation techniques, there is a tremendous amount of motivation and incentive in using

average power tracking and envelope tracking as viable solutions to the PA efficiency problem. With regards to the power amplifier, the use of CMOS technology provides a foundation for future research that will attempt to propose a monolithic IC solution of the PA and supply modulator.

1.4 Thesis Outline

This thesis is organized as follows. Chapter 1 discusses various efficiency enhancement techniques proposed over the years. In addition, the WCDMA and LTE wireless communication standards are introduced, and the PA compliance specifications are described.

Chapter 2 presents the design of a CMOS power amplifier that employs a TQFN package model and all integrated and off-chip passive devices. The design and simulation of the PA are performed using Agilent's Advanced Design System (ADS) [21].

Chapter 3 presents the behavioral modeling of envelope and average power tracking, and the impact that they have on the performance of the CMOS PA. A comparison is conducted between WCDMA and LTE applications.

Chapter 4 concludes the thesis. The main contributions of the thesis are summarized, and conclusions are presented based on the results obtained from the study. Trends and challenges that WCDMA and LTE signals impose on the designed CMOS power amplifier are also discussed.

Chapter 2

CMOS Power Amplifier

2.1 Introduction

This chapter will begin with a summary of the different linear power amplifier classifications. Key characteristics that define the performance of PAs will be explained, followed by a discussion of the limitations that CMOS has on the design of PAs. A design of a CMOS PA will be presented. The design employs BSIM3 transistor models and includes losses of passive elements. A detailed package model is employed to allow for a realistic estimate of efficiency performance.

2.2 Power Amplifier Classes

Power amplifiers can be classified either as bias dependent (Class A, AB, B, C), or based on switching devices, that depend on the frequency elements in the output matching network that shape the drain voltage and current signal (Class D, E, F) [2]. The PA classes in the latter group can theoretically achieve 100% efficiency assuming an ideal controlled switch (zero on-resistance, infinite off-resistance, zero transition time). For supply-tracking applications, a very linear device is required, while these switching devices

exhibit significant non-linearity. Therefore, a more suitable mode of operation would be to operate the transistor as a current source and provide linear amplification, which occurs in classes A, AB or B.

Table 2.1 [2] compares some of the linear power amplifier classes. In Class A amplifiers, the quiescent operating point is selected in the center of the linear region so that the drain current and voltage signals are completely sinusoidal. These amplifiers are continuously conducting and therefore rather inefficient. On the other hand, Class B amplifiers are biased at approximately zero quiescent current and hence only conduct for one-half of the cycle. These amplifiers trade off linearity for improved efficiency. Class AB operation offers a compromise between a highly linear Class A amplifier and more efficient Class B amplifier. In this thesis, a combination of Class A and Class AB amplifiers are utilized since linear operation is crucial for modulated envelope applications.

Table 2.1: Comparison of linear power amplifier classes.

Mode	**Bias Point** (V_g)	**Quiescent Current**	**Conduction Angle**	**Efficiency**	**Linearity**
A	0.5	0.5	2π	Poor	Excellent
AB	0-0.5	0-0.5	$\pi - 2\pi$	Fair	Good
B	0	0	π	Good	Fair

2.3 Characteristics of Power Amplifiers

The operation of any power amplifier is evaluated by several key performance characteristics. Understanding the significance of these characteristics

is an essential step before commencing the design of the PA. Section 2.3.1 will begin with an introduction to output power, gain, and efficiency. Section 2.3.2 summarizes both input/output signal linearity as well as system linearity specifications. Finally, in Section 2.3.3, several stability characteristics will be described that are useful for evaluating the robustness of the PA.

2.3.1 Output Power, Power Gain, and Efficiency

2.3.1.1 Output power

Output power is one of the most important characteristics in the design of a PA. It identifies the strength of the power level at an output load resistance of R, typically a 50Ω termination in RF applications. The output power for a sinusoidal signal can be expressed as:

$$Pout\,(W) = \frac{\left(\frac{V_{out-amplitude}}{\sqrt{2}}\right)^2}{R} \tag{2.1}$$

Usually power is defined as a decibel value with reference to 1mW

$$Pout\,(dBm) = 10log_{10}\left(\frac{Pout\,(W)}{1mW}\right) \tag{2.2}$$

2.3.1.2 Power gain

Power gain is an important metric, in addition to the output power, since it provides information about the input power required in order to generate a given output power. The three most widely used definitions for the power

gain of a PA are: Transducer Gain (G_t), Available Gain (G_a), and Operating Gain (G_o) [22]. They are defined as follows:

$$Transducer\ Gain\ (G_t) = \frac{Power\ at\ the\ load}{Maximum\ power\ from\ source} = \frac{P_{out}}{P_{Avs}} \tag{2.3}$$

$$Available\ Gain\ (G_a) = \frac{Maximum\ power\ out\ the\ PA}{Maximum\ power\ from\ source} = \frac{P_{Avo}}{P_{Avs}} \tag{2.4}$$

$$Operating\ Gain\ (G_o) = \frac{Power\ at\ the\ load}{Power\ into\ the\ PA} = \frac{P_{out}}{P_{in}} \tag{2.5}$$

In this thesis, the transducer gain will be used to represent the power gain.

2.3.1.3 Efficiency

The efficiency of a power amplifier is a very critical figure of merit (FoM) for mobile handsets. The goal of this thesis is to improve this performance metric through the implementation of supply-tracking techniques. However, before attempting to solve this power consumption problem, it is crucial to define and understand how to measure the efficiency of a PA.

Output power is produced by providing RF power to the input of the PA and an even higher amount of DC power through the supply. Any input energy that is not converted to output RF power is dissipated as heat. The most popular and accurate way to represent efficiency is in the form of power-added

efficiency (PAE), which is defined as the ratio of the difference between the output and input RF powers, to the DC power dissipation. This is very useful when evaluating a multi-stage PA that generates power gain by consuming a certain amount of power. For low gain PAs, the input power has a significant impact on efficiency. The PAE is given by

$$PAE\,(\%) = \frac{P_{out}(W) - P_{in}(W)}{P_{DC}(W)} * 100\% = \left(1 - \frac{1}{G}\right)\left(\frac{P_{out}(W)}{P_{DC}(W)}\right) * 100\% \quad (2.6)$$

To define the efficiency of a single stage and the quality of its output matching network, it may be useful to characterize the drain efficiency (η) instead.

$$\eta\,(\%) = \frac{P_{out}(W)}{P_{DC}(W)} * 100\% \quad (2.7)$$

2.3.2 Linearity

The linearity of a PA is an extremely important FoM, and it is defined in various ways. The relevant metric depends on features of the application such as the modulation scheme. This chapter is primarily focused on the design of power amplifier for operation with non-modulated CW inputs. First, the 1-dB compression point (P1dB), and third/fifth-order intermodulation distortion (IMD3, IMD5) will be discussed. Then, in Chapter 3, several other linearity criteria such as ACLR and EVM will be defined for complex modulated PA applications.

2.3.2.1 P1dB

When a single tone, $x(t) = Acos(\omega t)$, is applied to a PA, which is modeled as a nonlinear system $\{y(t) \approx \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 + ...\}$, the following output is generated

$$\begin{aligned} y(t) &\approx \alpha_1[Acos(\omega t)] + \alpha_2[Acos(\omega t)]^2 + \alpha_3[Acos(\omega t)]^3 \\ &= \frac{1}{2}\alpha_2 A^2 + (\alpha_1 A + \frac{3}{4}\alpha_3 A^3)cos(\omega t) + \frac{1}{2}\alpha_2 A^2 cos(2\omega t) \\ &\quad + \frac{1}{4}\alpha_3 A^3 cos(3\omega t) \end{aligned} \tag{2.8}$$

The output consists of a DC component, fundamental frequency component at ω and higher-order harmonics (2ω and 3ω) as shown in (2.8). The amplitude of the fundamental component is strongly affected by the third-order nonlinearity coefficient α_3, and its sign depends on whether the output is compressing ($\alpha_3 < 0$) or expanding ($\alpha_3 > 0$) with an increase in input. The 1-dB compression point is defined as the location at which the linear gain drops by 1dB. This point can be determined by plotting the power transfer function (Pout vs. Pin), however a simpler approach is to plot the gain transfer function (Gain vs. Pin).

2.3.2.2 IMD

Intermodulation distortion also arises from the above non-linearity and requires the presence of multi-tone inputs. Its origin can be understood using

a multi-tone nonlinearity analysis. Assuming two signals with equivalent amplitudes, $x(t) = Acos(\omega_1 t) + Acos(\omega_2 t)$, are applied to the same nonlinear PA model, the output becomes

$$y(t) = (\alpha_1 A + \frac{9}{4}\alpha_3 A^3)cos(\omega_1 t) + (\alpha_1 A + \frac{9}{4}\alpha_3 A^3)cos(\omega_2 t) + \frac{3}{4}\alpha_3 A^3 cos(2\omega_1 - \omega_2) + \frac{3}{4}\alpha_3 A^3 cos(2\omega_2 - \omega_1) + ... \quad (2.9)$$

The third-order intermodulated terms (IMD3) appear very close to the fundamental components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. From (2.9), IMD3 amplitude increases three times as fast as the fundamental amplitude in a decibel scale. Similarly, the fifth-order intermodulated terms (IMD5) appear at $3\omega_1 - 2\omega_2$ and $3\omega_2 - 2\omega_1$ with a slope of five times that of the fundamental gain slope in a decibel scale.

2.3.3 Stability

PA stability is a significant design consideration. An ill-designed PA can become unstable and oscillate. Many different methods can be employed to analyze stability and verify functional operation. In this section, an introduction to stability will be presented. Some of the key causes of instability in power amplifiers will be mentioned and several ways of analyzing and simulating stability will be discussed.

2.3.3.1 Sources of instability

There are many contributing factors in the design of a PA that can render it unstable. Some of the most common reasons are listed below.

- Feedback-induced instability can occur through the ground connections especially when cascading multiple stages [23]. In practice, the ground nodes are not connected to ideal ground, but through bondwires internal to the package and then connected to an off-chip ground. These bondwires have a big impact on the gain and stability of the power amplifier. A feedback path can be formed from output to input through the ground connections. With sufficiently large loop gain in a single stage, oscillations can appear [24]. These harmful feedback loops can also occur at other nodes such as the output, supply and bias locations.

- Mutual coupling effect between inductors is another potential cause of instability. This coupling effect could result from sub-optimal layout. Improper placement of passive devices may decrease the isolation between input and output. For example, when routing two inductors in the same direction, their mutual effect is maximized, and a loop is created between those two portions of the circuit [25].

2.3.3.2 Stability analysis and simulations

The study of stability can be divided into two categories: linear and non-linear analysis. The efficacy and limitations of each method are summa-

rized below [25].

- **Linear analysis**: it consists of a 2-port examination that involves the calculation of S-parameters. The K-factor is used as the stability criterion and must satisfy the following condition in order for the PA to be considered unconditionally stable:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \tag{2.10}$$

$$where\ \Delta = S_{11}S_{22} - S_{12}S_{21} > 1 \tag{2.11}$$

In practice, stability must not only be assured at the operating frequency but over all frequencies and combinations of source and load impedances (Z_S, Z_L). A key limitation in this analysis is that K-factor is only calculated for a specific combination of Z_S and Z_L. One solution would be to sweep (Z_S, Z_L) through load-pull simulations and plot stability circles on Smith charts. A linear stability analysis is sufficient for a small-signal regime. However, since the PA will be operating in the large signal domain, a non-linear analysis of the PA is required as well.

- **Non-linear analysis**: a Harmonic Balance (HB) simulator provides a non-linear analysis of power amplifiers. Measuring current, power and distortion in the frequency domain can provide good intuition into the non-linear performance and stability of the PA. The main limitation of

HB simulations is that the PA is excited with an ideal CW signal at a fixed frequency and not over a wide range of frequencies.

Some of the causes of instability that are mentioned in this section are observed during the design of the CMOS PA in this thesis. The solutions to avoid unstable behavior will be proposed. In addition, both a linear and non-linear analysis of the PA will be conducted. Small-signal S-parameters will be simulated to plot K-factor from DC to 10GHz. However, the stability will be verified for only 50Ω terminations at the source and load. Furthermore, a variety of HB simulations will be conducted to fully characterize the large signal performance of the PA[1].

2.4 Limitations of CMOS Power Amplifiers

The two major limitations that are observed in this CMOS design are low breakdown voltage and low transconductance-to-current ratio [23].

2.4.1 Low Breakdown Voltage

Oxide breakdown occurs in a MOSFET if a large voltage is applied to the gate. As a result, a short circuit is formed between the gate and the channel through the oxide which can be very destructive to the transistor. A reduction in CMOS technology size can be beneficial in allowing for new methods of implementation and increased performance. However, as this technology

[1]The stability of the PA while being driven with modulated signals is not analyzed.

shrinks, the gate thickness decreases as well, and the maximum allowable gate voltage is further limited.

There are other forms of breakdown that occur within a MOSFET [26]. The first type can arise between the drain to substrate p-n junction. A large current is produced if the applied drain voltage is too high. This is known as *weak avalanche*. Secondly, as the size of the device becomes smaller, *punch-through* breakdown can become significant. When the drain voltage becomes too large, the depletion region around the drain extends completely through the channel to the source terminal. This also results in a rapid increase in the drain current. Even though these breakdown effects are nondestructive, they limit the maximum PA voltage swing at the drain of the device.

2.4.2 Low g_m/I ratio

Another major limitation found in CMOS devices is their inherently smaller transconductance-to-current ratio compared to other technologies such as III-V or bipolar. Therefore, power amplifiers designed in CMOS must consume more current to achieve the same g_m. To accommodate for low g_m, either the CMOS transistor size or the input signal amplitude must be increased. The latter approach degrades the linearity of the PA since the third-order nonlinearity component is directly proportional to the cube of the input amplitude and degrades power-added efficiency.

2.5 Design and Modeling of Linear CMOS PA

This section discusses the design and optimization of a CMOS PA including the modeling of the inductor and capacitor lumped elements and package. Simulation results demonstrate a functional CW (continuous-wave) design that is a good candidate for both WCDMA and LTE supply-tracking applications. An output 1-dB compression point (OP1dB) of 27.4dBm and a PAE of 36.4% is achieved in a fixed 3.7V supply operation. The critical design issues that were encountered are mentioned and their impact on performance is discussed.

A common design methodology found in literature [25, 23] is chosen for the design of this PA. The proposed process is as follows:

1. PA Architecture:
   (a) Choice of configuration
   (b) Transistor topology
   (c) PA class of operation
2. Design Power Stage:
   (a) Load-pull, Z_{opt} determination
   (b) Transistor sizing and biasing
   (c) Output matching network
   (d) Check for stability and adjust matching

3. Design Driver Stage:

   (a) Transistor sizing and biasing

   (b) Interstage matching

   (c) Check for stability and adjust matching

4. Add Lumped Element and Package Models:

   (a) Inductor and capacitor models

   (b) Generation of package model

   (c) Check for stability and adjust matching

2.5.1 PA Architecture

Defining the architecture to meet the target output power and linearity specified in Chapter 1 is the first step in the PA design process. For simplicity, a single-ended configuration is utilized since this study is focused on the behavior of a stand-alone PA. To prevent excessively large power gain in a single stage that can potentially lead to instability, a two-stage structure is proposed to distribute the gain. As shown in Figure 2.1, the PA consists of: a power stage, a driver stage, bias circuitry, and impedance matching networks.

The two most common transistor topologies are the common source (CS) and cascode. The cascode structure is beneficial in providing higher gain and improved reverse isolation from output to input by mitigating the effect of the Miller capacitance C_{gd}. Secondly, it allows for the use of smaller transistors

by relaxing the breakdown voltage concerns. However, this architecture has a limited range of voltage swing at the drain of the output device which results in smaller linear output power and efficiency. Also, the inclusion of the common-gate (CG) transistor in the cascode topology introduces additional parasitics and nonlinearity, which complicates the design of the PA.

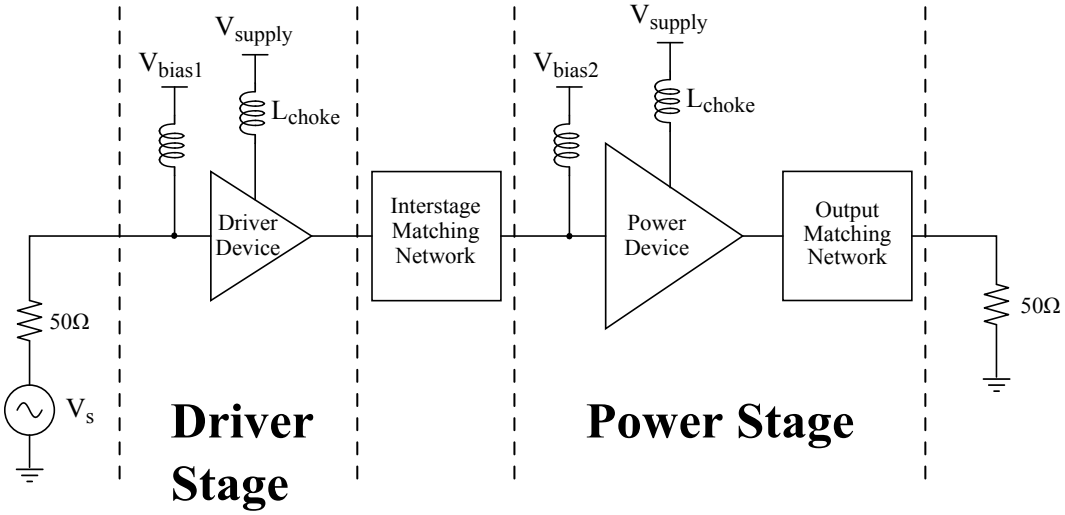

Figure 2.1: High level block diagram of a single-ended, two-stage PA structure.

Even though the CS structure suffers from lower gain and poor isolation and stability, the key advantages (higher linearity, Pout, and efficiency) can outweigh the disadvantages. Thus, a single-transistor, CS configuration is chosen in this design. In order to provide the required output power, a nominal supply of 3.7V was found to be suitable. To operate with this supply, both the power stage and driver stage consist of thick gate-oxide NMOS devices with sufficiently high breakdown voltage and a channel length of $0.34\mu m$.

The PA class of operation is controlled by biasing conditions as well as

any frequency-dependent circuitry such as the matching networks and package parasitics. Determining the mode of operation strongly depends on which system requirements are priorities. As mentioned previously (in Chapter 1), envelope tracking for WCDMA or LTE applications requires a linear PA that can withstand being driven with significant amplitude modulation. A combination of class A and class AB stages are used to optimize both the linearity and efficiency. In the upcoming sections, the choice of operation for each stage will be defined. Throughout the design process, the adjustment in biasing is iterative.

2.5.2 Power Stage Design

As previously illustrated, the PA design progresses from output to input. The power stage is considered the "power hungry" portion of the PA since it must provide high output power to the antenna. There are many critical tradeoffs that occur between linearity, gain and PAE in this stage. Consequently, there exists a high degree of difficulty in locating the optimum point of operation and this is what makes the design of the power stage the most challenging step in the design process. This section is divided into three parts as follows:

- Load-pull characterization and determination of optimum load impedance (Z_{opt})
- Load impedance adjustment

- Off-chip output matching network design

2.5.2.1 Load-pull characterization and determination of optimum load impedance (Z_{opt})

To understand the power delivery capability of the power device by itself, load-pull analyses were performed. In order to provide over 24dBm linear output power, the location of P1dB is selected around 28dBm. The power stage is chosen to operate in class AB mode to balance efficiency and linearity. Assuming a drain efficiency of approximately 60%, $V_{DD} = 3.7$V, and $P_{out} = 28$dBm, the DC current is calculated to be approximately 250mA using (2.12).

$$\eta = \frac{P_{out}}{V_{DD} I_{DD}}$$

$$\Rightarrow I_{DD} = \frac{P_{out}}{\eta V_{DD}} \tag{2.12}$$

The power transistor must be sized to generate the desired output power and ensure that the output stage does not drift too far from the desired class AB mode. There are several adjustable parameters that modify the sizing of the transistor: the finger width (W_f), the number of fingers (N_f) and the number of transistor cells in parallel (M), where the effective width is $W_{eff} = W_f \cdot N_f \cdot M$. There are limitations on W_f and N_f and the effective size can be realized with different combinations for the three parameters.

The power amplifier does not use conjugate matching at the output to optimize gain as in the design of low noise amplifiers (LNA). Instead one of the most popular approaches for designing power amplifiers is utilizing the load-pull methodology to determine, Z_{opt}. With the use of a load tuner, a variation in load reflection coefficients results in a range of output impedance, $Z_L = (R_L + jX_L)$. Maximum power and efficiency is observed at Z_{opt}. The overall power, efficiency and linearity performance can be measured for specific simulated load impedances.

In this study, load-pull simulations are conducted specifically to size the power device for optimal $P1dB$, P_{del} (power delivered), and PAE, while achieving adequate $IMD3, IMD5$. First, a two-tone simulation is conducted. As shown in Table 2.2, optimal P_{del} and PAE are achieved through choice of $\{W_f, N_f, M\}$ using a fixed bias V_{GS} of 1.2V at a load impedance of $Z_L = 11.71 + j12.47\,\Omega$. Sufficiently low IMD3 and IMD5 are achieved.

Table 2.2: Optimized two-tone load-pull simulation results.

V_{GS} (V)	1.2
V_{DD} (V)	3.7
I_{DC} (mA)	243
W_{eff} (μm)	1920
P_{del} (dBm)	24.62
$PAE_{@\,Pdel}$ (%)	27.71
$\{IMD3, IMD5\}_{@\,Pdel}$ (dBc)	{-42, -31}
$Z_L = (R_L + jX_L)$ (Ω)	$11.71 + j12.47$

Note: Pin1 = Pin2 = 10dBm, tone spacing = 5MHz.

Next, a one-tone simulation is conducted to optimize the 1dB gain compression output power and PAE as displayed in Table 2.3. As the biasing is increased, the transistor is pushed further into the class A regime, and the PAE is reduced. On the other hand, as the biasing is reduced, a significant drop in $P1dB$ is observed. Therefore, a gate biasing of 1.2V is chosen as the best compromise between high P1dB and PAE.

Table 2.3: Optimized one-tone load-pull simulation results.

V_{GS} (V)	1.2
V_{DD} (V)	3.7
I_{DC} (mA)	243
W_{eff} (μm)	1920
$P1dB$ (dBm)	28.05
$PAE_{@P1dB}$ (%)	58.01
$Z_L = (R_L + jX_L)$ (Ω)	$11.71 + j12.47$

Note: Pin = 10dBm.

The load-pull approach is very helpful in providing a quick understanding on how the operating conditions affect performance. However, adjusting the sizing or biasing along the design flow requires re-characterization of the transistor and is an iterative process.

2.5.2.2 Load impedance of final PA

Through extensive simulations of the final PA that include observations from load-pull analysis of the power device, DC to RF behavior, and optimizing efficiency and output power, it was found that a load impedance of $7.4 + j9.7\ \Omega$

provides adequate performance for the application that is discussed in Chapter 3.

2.5.2.3 Off-chip output matching network design

It should be noted that the load impedance is **not** conjugate matched to the output impedance of the power stage, $Z_L \neq Z_{out-pwr*}$. Since maintaining power gain in CMOS PAs is a difficult task, an off-chip output impedance transformation network is implemented to minimize any additional power loss. The 50Ω antenna impedance (Z_A) is transformed to a lower load impedance

$$Z_L = R_L + jX_L \tag{2.13}$$

through a single section low-pass network as shown in Figure 2.2.

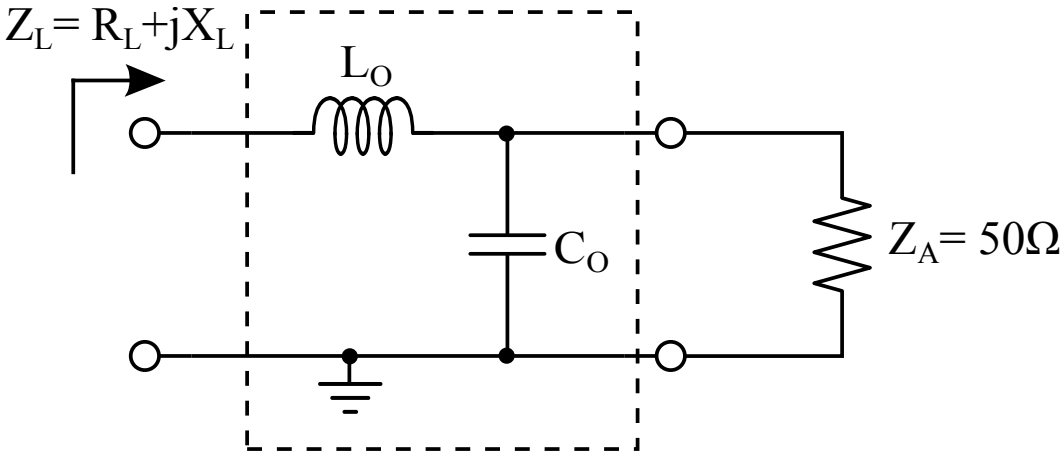

Figure 2.2: Lumped-element low-pass network.

The impedance looking into the impedance transformation network

consists of a capacitive reactance shunting the antenna along with a series resonant inductive reactance [2, 22], *i.e.*,

$$Z_L = Z_{Lo} + Z_{Co} \,||\, (Z_A) = Z_{Lo} + \frac{Z_{Co} Z_A}{Z_{Co} + Z_A} \tag{2.14}$$

where $Z_{Lo} = jX_{Lo}$, $Z_{Co} = jX_{Co}$, and $Z_A = R_A$.

By inserting (2.13) into (2.14), the following solutions are determined:

$$X_{Co} = -\frac{R_A}{\sqrt{m-1}}$$

where the transformation ratio is $m = \dfrac{R_A}{R_L}$.

$$\Longrightarrow \qquad C_o = \frac{-1}{\omega X_{Co}} \tag{2.15}$$

$$X_{Lo} = (X_L + R_L\sqrt{m-1})$$

$$\Longrightarrow \qquad L_o = \frac{X_{Lo}}{\omega} \tag{2.16}$$

The design of the power stage is shown in Figure 2.3. The elements in the output matching network create a desired load impedance of $7.4 + j9.7\ \Omega$ at the fundamental frequency of $f_1 = 1950$MHz. The actual implementation of the passive elements including the modeling of the parasitics is presented in Section 2.5.4.

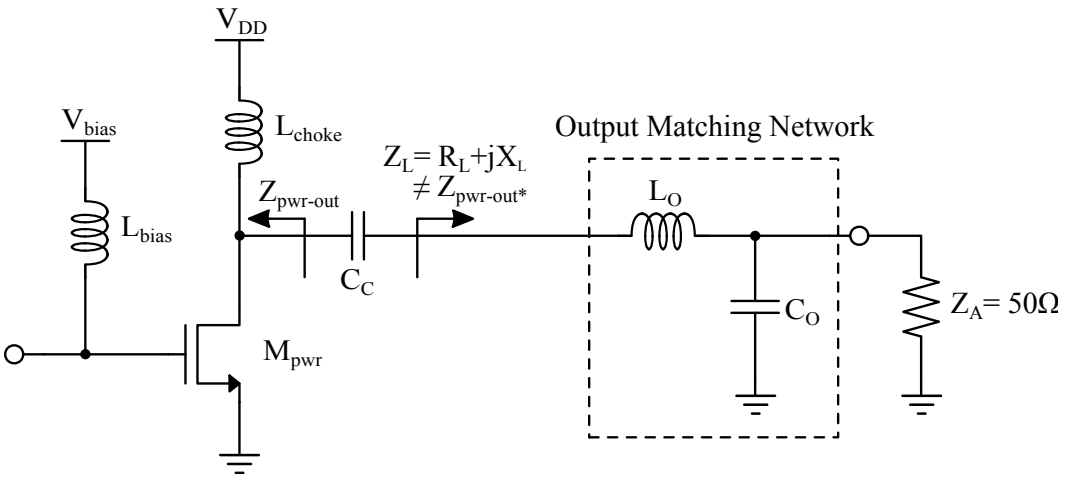

Figure 2.3: Design of power stage including output matching network transforming 50Ω to $7.4 + j9.7\ \Omega$ (parasitics not shown).

2.5.3 Driver Stage Design

The driver stage provides an additional gain stage at a cost for overall efficiency reduction. In comparison to the power stage, the size of the driver transistor is scaled to $1280\mu m$ and biased at 0.85V since the output stage has more bearing on the overall linearity of the PA than the input stage. As shown in Figure 2.4, a shunt feedback network is used for the driver stage. This topology is chosen for gain and stability purposes more so than for broadband

matching. A large 120Ω resistor is selected as the optimum value for good gain and sufficient feedback for stability.

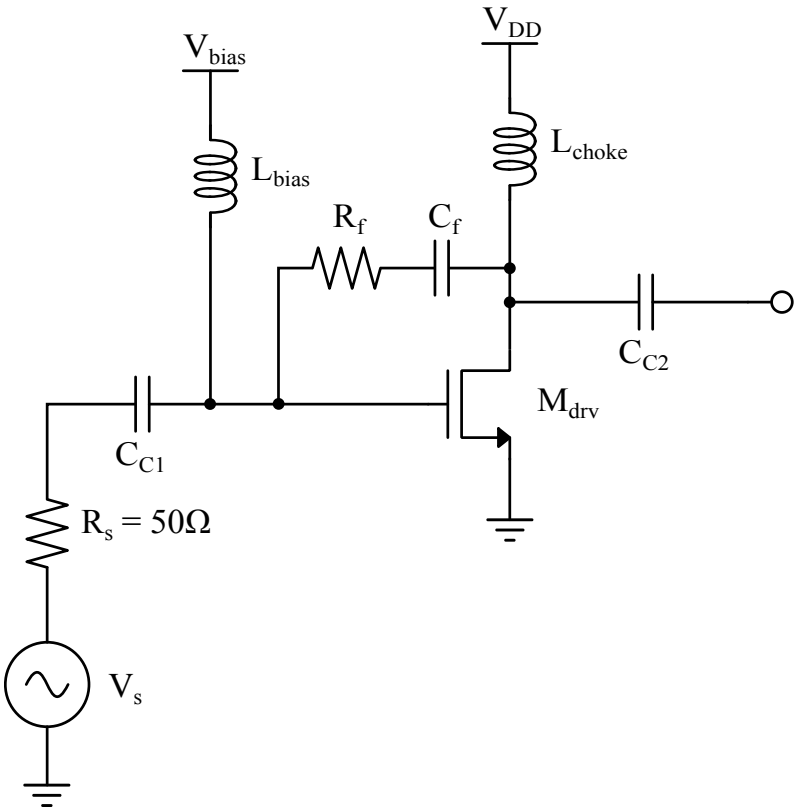

Figure 2.4: Driver stage including resistive shunt feedback network.

2.5.3.1 Input Matching

To improve performance using an input match, it was observed that high-Q, ideally lossless passive elements were required. For the intended application, however, the use of off-chip passive matching elements was avoided on the input. Since the loss of on-chip elements was found to negate any potential improvement through matching, an explicit input matching network

is avoided. Through careful simulations, it is determined more beneficial to utilize only an interstage matching network and not employ an explicit input matching network.

2.5.3.2 Interstage Matching

An interstage matching network is placed in between the driver and power stages to maintain gain and efficiency through the RF signal path. The design methodology is referenced from [23] and is based off the *maximum power transfer theorem*, which matches the input impedance of the power stage to the complex conjugate of the output impedance of the driver stage. The traditional conjugate-match analysis is only valid assuming that the matching network is lossless, which is not the case with on-chip passive elements. The complete analysis, considering the parasitic loss in the interstage matching network, is found in [23].

As shown in Figure 2.5, the input impedance of the power transistor is modeled as a parasitic gate resistance, Rg_{pwr}, in series with a gate capacitance, Cg_{pwr}. The output impedance of the driver transistor is modeled as the channel-length modulation resistance, Rds_{drv}, in parallel with the total drain capacitance, Cd_{drv}. The interstage matching network consists of a shunt inductor, L_{int}, and a DC-blocking capacitor, C_{int}. Let C_{tot} represent the series summation of C_{int} and Cg_{pwr},

$$C_{tot} = \left(\frac{1}{C_{int}} + \frac{1}{Cg_{pwr}} \right)^{-1}, \tag{2.17}$$

where the quality factor of C_{tot} is

$$Q_c = \frac{1}{\omega R g_{pwr} C_{tot}}. \tag{2.18}$$

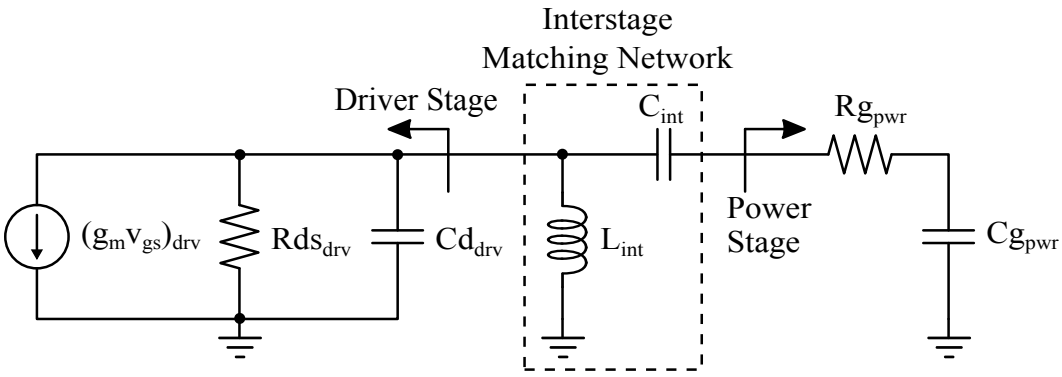

Figure 2.5: Interstage matching network (parasitics not shown).

The power transferred to Rg_{pwr} is derived by transforming the circuit in Figure 2.5 into a RLC parallel network to take advantage of the simplicity of admittance. For maximum power transfer to Rg_{pwr}, the partial derivative of the power transfer function is first taken with respect to Q_c and next with respect to L_{int}. The optimum values of Q_c and L_{int} are determined as

$$Q_c = \sqrt{\left(\frac{1}{Rg_{pwr}\left(\frac{1}{Rds_{drv}} + \frac{\omega C d_{drv}}{Q_L}\right)}\right)} \tag{2.19}$$

$$L_{int} \approx \left(\frac{Q_c R g_{pwr}}{\omega(1 + \omega Q_c R g_{pwr} C d_{drv}}\right), \tag{2.20}$$

where Q_L is the quality factor of L_{int}.

C_{tot} can be calculated by inserting (2.19) into (2.18) and finally, C_{int} is calculated by inserting (2.18) into (2.17). In this study, the integrated inductors used have a Q_L of approximately 8.

2.5.4 Lumped-Element Models

All the integrated (inside red dashed line) and off-chip passive elements used in the design are labeled below.

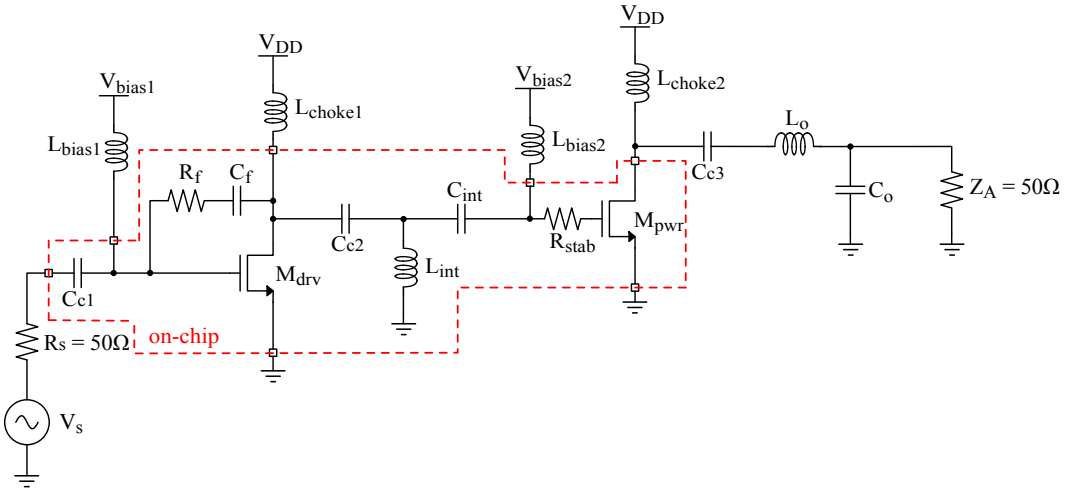

Figure 2.6: Complete two-stage PA design.

2.5.4.1 Inductors

The only integrated inductor used in this design is located in the interstage matching network (L_{int}). All remaining inductors are RF surface mounted in the form of lumped-element (SPICE) models. All off-chip inductors are assumed to be of very high Q. Table 2.4 summarizes the inductance

values utilized in the simulation. The off-chip inductors have a Q in excess of 80, while the integrated inductor has a Q of approximately 8. The majority of the parasitic loss arises from the on-chip matching network due to low Q integrated passive elements. This is justified through simulation in Section 2.5.8.

Table 2.4: Assumed values of off-chip and integrated inductors at f_1 = 1950MHz.

Inductors	**L(nH)**
Off-chip output choke (L_{choke2})	15
Off-chip input choke (L_{choke1})	12
Off-chip output matching (L_o)	2.2
Integrated interstage matching (L_{int})	2.6

2.5.4.2 Capacitors

The output DC blocking capacitor (C_{c3}) and output matching capacitor (C_o) are assumed to be off-chip and employ practical device models with a Q factor in excess of 100. The remaining capacitors (C_{c1}, C_{c2}, C_{int} and C_f) are integrated and have significantly smaller Q factor of approximately 10.

Table 2.5: Values of off-chip and integrated capacitors at f_1 = 1950MHz.

Capacitors	**C(pF)**
Off-chip output matching (C_o)	3.9
Integrated feedback (C_f)	6
Integrated DC blocking (C_{c1}, C_{c2})	10
Off-chip DC blocking (C_{c3})	7
Integrated interstage matching (C_{int})	3

2.5.5 Package Model

To provide a more accurate simulation of the PA circuit, a TQFN (thin quad flat no leads) package model is generated with the support of a tool provided by Maxim Integrated Products (Figure 2.7). A configuration of two bondpads per leadframe pin is used to decrease the impedance path. This is critical for the ground pins where a large amount of source degeneration can greatly reduce the gain. A total of six bondpads and three leadframe pins are used for Gnd1 (driver stage ground) and Gnd2 (power stage ground) to maintain gain. Four bondpads per two leadframe pins are used for Vdd2 (same as RFout) since the output matching network is very sensitive to inductive variations.

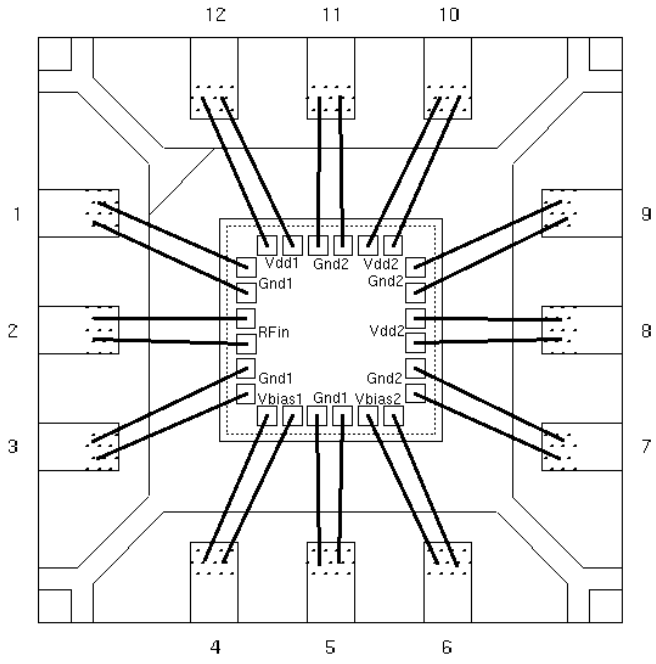

Figure 2.7: TQFN package model.

The package model consists of a very thorough representation of bondwire parasitics and the mutual coupling effect between inductors. An equivalent model of the bondpad-to-leadframe parasitics is shown in Figure 2.8. These bondwires can degrade the large signal performance, if the desired load impedance is not properly realized. The impact that the package elements have on performance is discussed in Section 2.5.8.1.

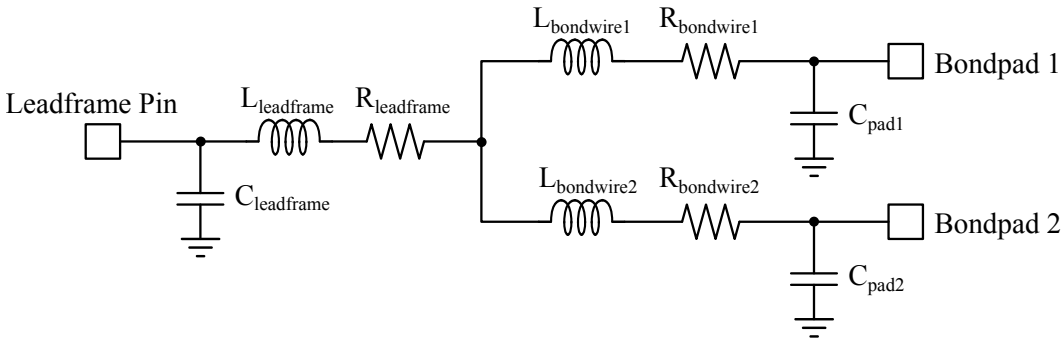

Figure 2.8: Two bondpads per leadframe pin configuration.

2.5.6 Simulation Tools for PA Design

Harmonic balance (HB) approach is employed to simulate the nonlinearity behavior of the PA and evaluate both total harmonic distortion (THD) and intermodulation distortion (IMD) components. This frequency-domain approach can easily sweep the real and imaginary components of the reflection coefficient and perform load-pull contour analyses. DC simulation is employed to characterize the device and optimize its operating point.

- DC (IV characteristics, power consumption)

- Harmonic balance
  - One-tone (Pout, Gain, PAE) vs. Two-tone (IMD)
- S-parameter
  - S11, S12

2.5.7 Stability

As is crucial in the design of any analog/mixed-signal circuit, the stability of the PA is constantly monitored throughout the design process. Several key design parameters are adjusted, mainly due to the strong influence that they have on stability.

The range of stability depends on the application in which the PA is being used. In this case, the PA must be able to endure supply modulation in the range of 1.3V to 3.7V for average power tracking. Furthermore, envelope tracking will modulate the PA with an envelope which will consist of a similar average supply voltage dynamic range. Normally, a reduction in gain is a simple cure to stabilizing a PA through the use of a series resistance at the gate of the power stage [24]. Figure 2.9 shows the small-signal K-factor stability curves for different series resistances.

A resistance of 24Ω is selected to achieve K-factor > 1 over frequency and supply as shown in Figure 2.10. To a first degree, the stability of the PA is established over a wide operating range.

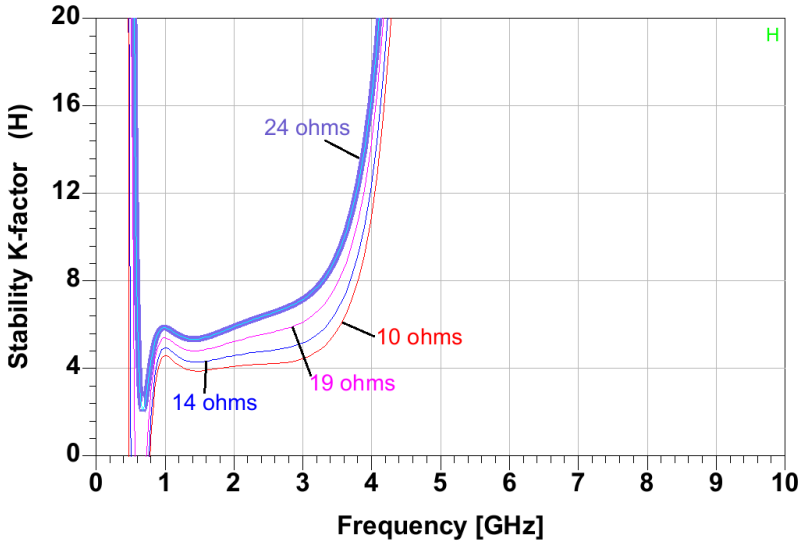

Figure 2.9: Simulated K-factor stability for varying series resistances at a reduced supply voltage of 2.7V.

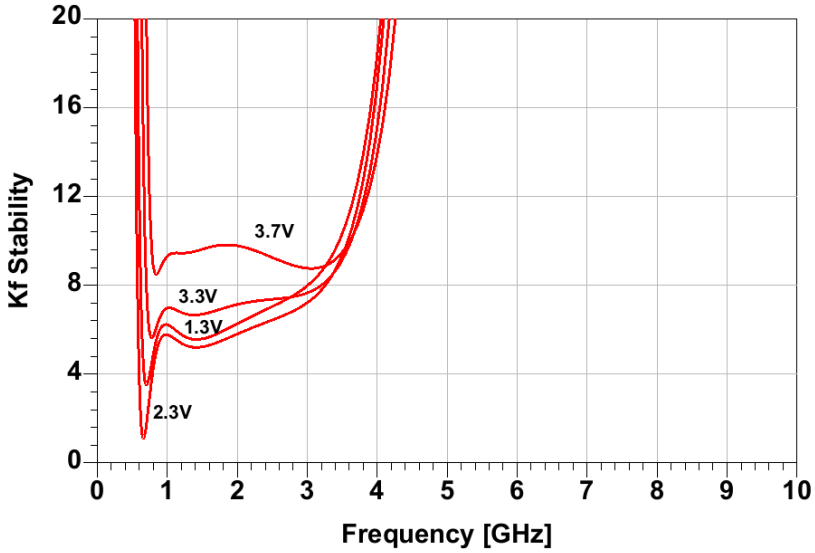

Figure 2.10: Simulated K-factor over supply voltage for a series resistance of 24Ω.

2.5.8 Final Design and Performance

In this section, a summary of the single-tone and two-tone simulation results is presented.

2.5.8.1 Single-tone simulation results

The large signal gain and PAE performance is plotted in Figure 2.11. Driving the PA with a CW input and a supply voltage of 3.7V, a gain of 15.5dB with an output P1dB of 27.4dBm is achieved. The PAE at P1dB is 36.4%, however it drops off a considerable amount in back-off power regions.

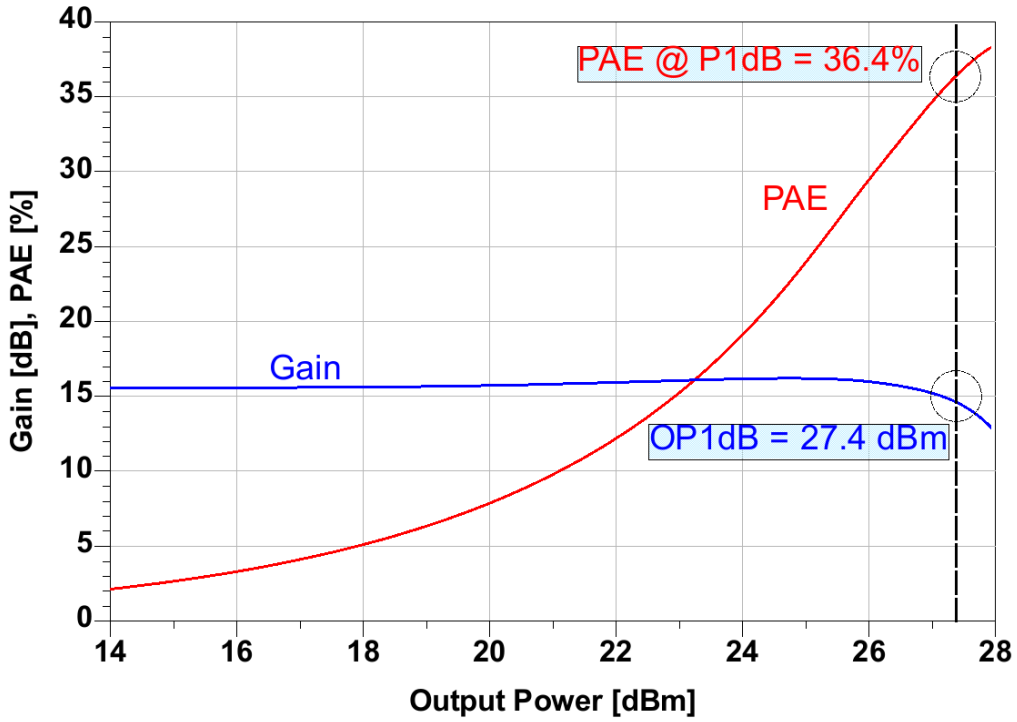

Figure 2.11: Simulated transducer gain and PAE for a 1950MHz CW input and nominal 3.7V supply.

Figures 2.12 and 2.13 display the effect that the parasitics in the package and lumped element models has on the gain and efficiency performance. The following four scenarios are analyzed:

- Ideal PA (no package, no inductor/capacitor parasitics)
- Inductor/capacitor parasitics only
- Package only
- Final PA (package and inductor/capacitor parasitics modeled)

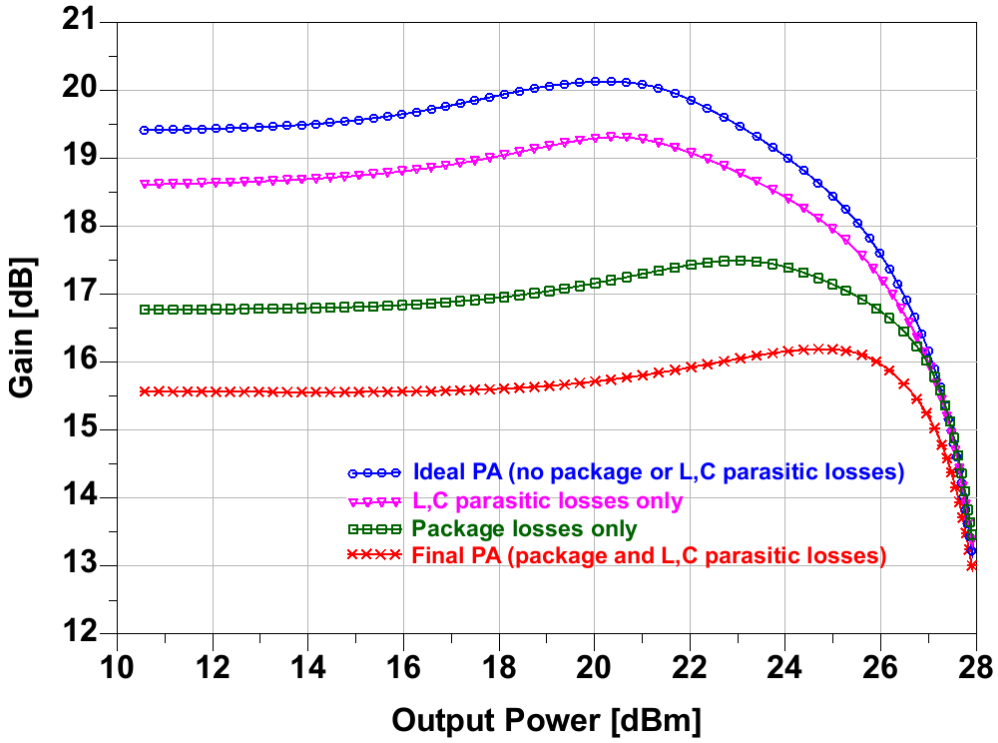

Figure 2.12: Gain reduction in the package and lumped element models.

As shown in Figure 2.12, a total of 3dB gain is lost due to parasitics in the package, most of which is due to the large amount of source degeneration in the GND paths. This includes the placement of multiple GND bondpads to reduce the effective size of the bondwires by a factor of 3. Hence, the 1-dB compression point is extended and the PA benefits from additional linearity. The integrated inductors and capacitors reveal another 1dB of gain reduction and an efficiency degradation of 2.5% at P1dB (Figure 2.13). All high-Q off-chip elements have minimal impact on the gain and efficiency. Also, a power loss of 1dB is observed from the RF power source to the PA input due to input mismatch.

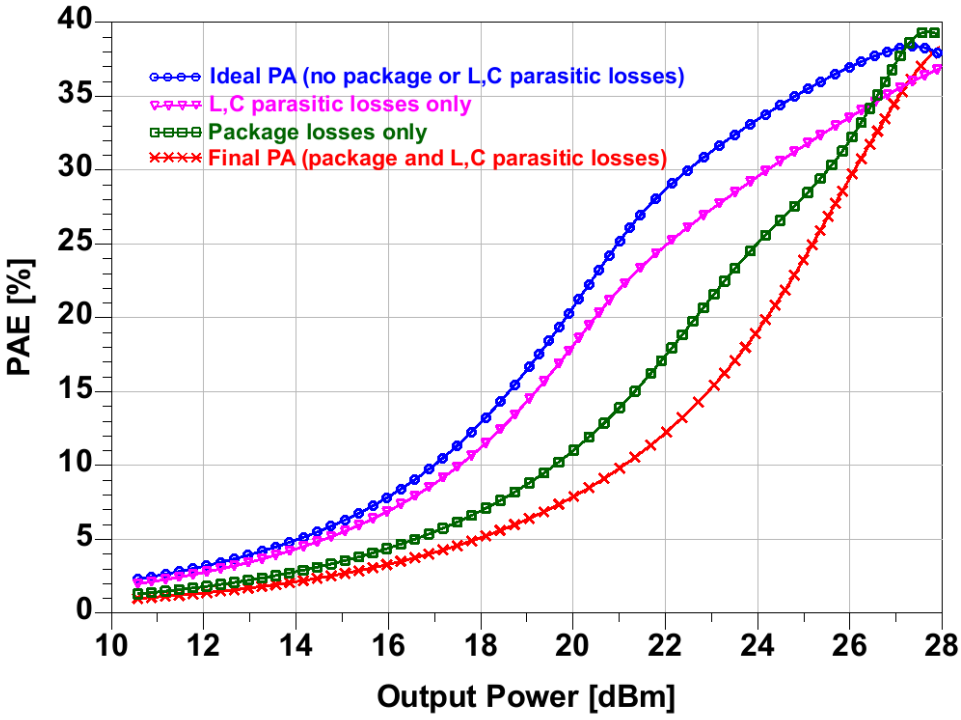

Figure 2.13: Efficiency loss in the package and lumped element models.

2.5.8.2 Two-tone simulation results

A two-tone simulation is performed to analyze the intermodulation distortion of the PA. The expansion behavior noticed in the gain plots of Figure 2.12 is considered a form of gain compression cancellation, also known as predistortion, and therefore creates deep notches in the IMD response. This third-degree expansion is often an inherent characteristic of the FET devices when operating at a lower bias regime [27]. In Figure 2.14, the IMD3 notch occurs as the gain of the PA is beginning to expand.

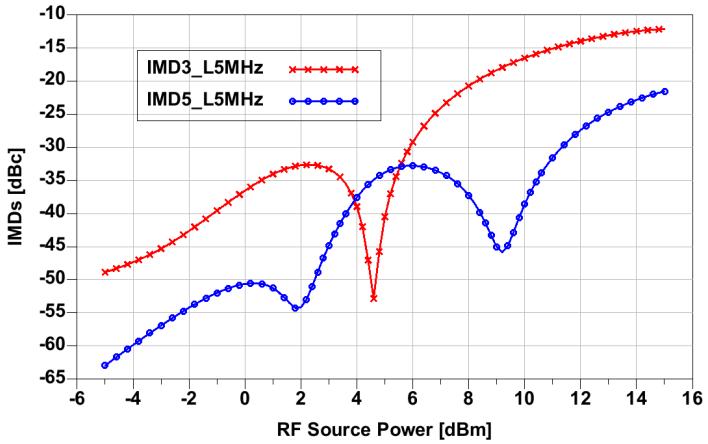

Figure 2.14: Simulated IMD3, IMD5 for 3.7V supply (5MHz tone spacing).

As the PA supply will be modulated down to lower voltages in power and envelope tracking, the IMD response over supply must also be carefully examined. As displayed in Figures 2.15 and 2.16, the gain expansion behavior disappears with a reduction in supply. As will be presented in the next chapter, this will set a lower limit on the supply in which the PA stays within range of

meeting the system linearity requirements.

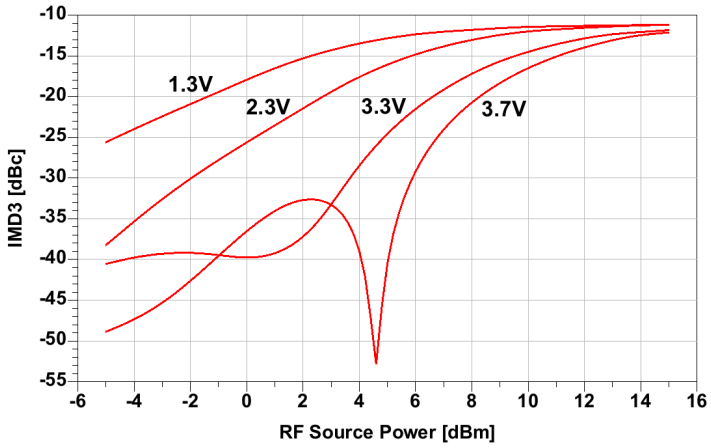

Figure 2.15: Simulated IMD3 over supply.

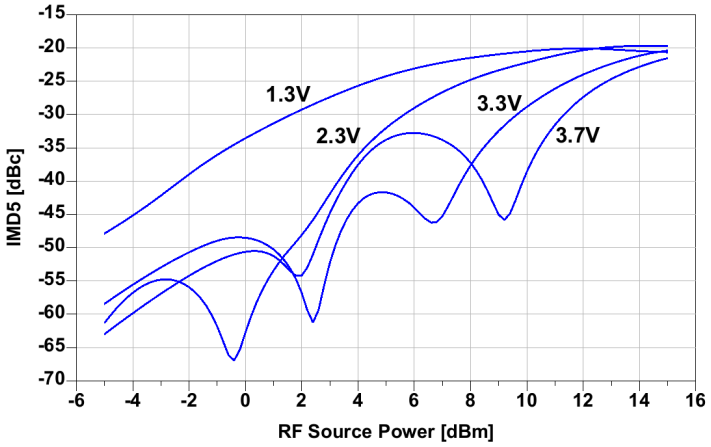

Figure 2.16: Simulated IMD5 over supply.

The current and voltage waveforms are plotted in Figures 2.17 and 2.18 for single-tone input power levels -5, 5 and 10dBm. The effective operation of the designed two-stage PA is Class A/AB. The driver stage conducts 100% of

the time while the power stage conducts 87% of the time. A very linear PA is required for WCDMA and LTE characterization.

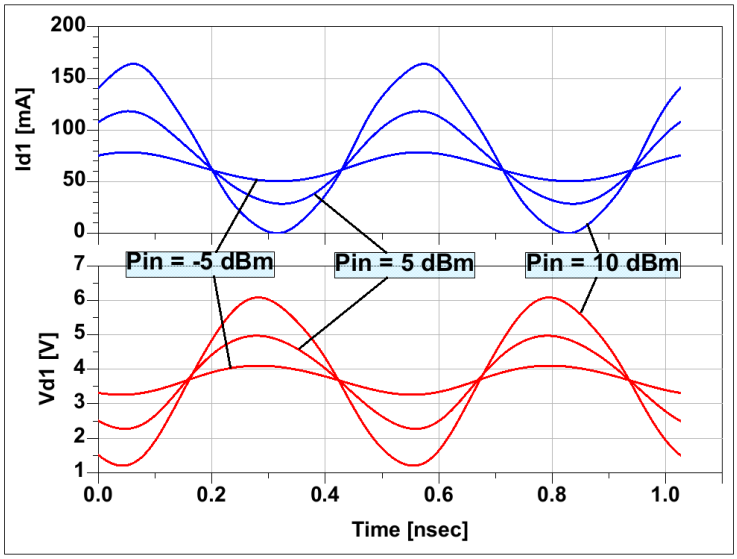

Figure 2.17: Current and voltage waveforms of driver stage.

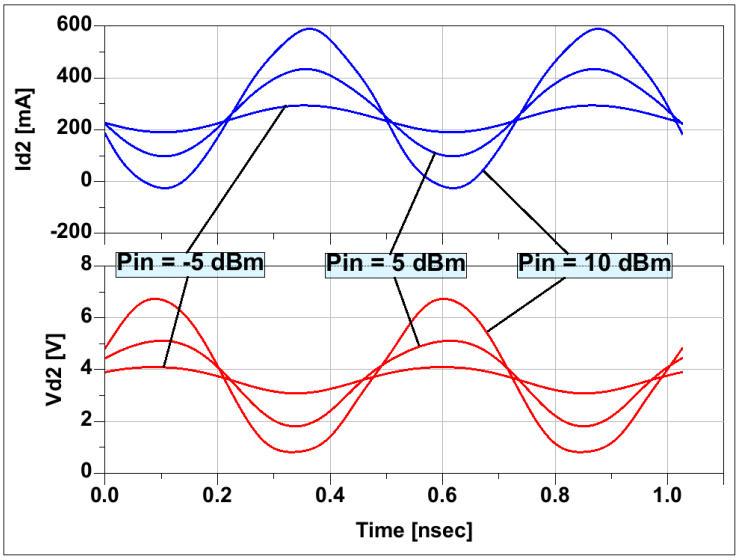

Figure 2.18: Current and voltage waveforms of power stage.

2.6 Conclusion

This chapter commenced with an introduction of the important RF characteristics that define the operation of a power amplifier. Also several of the linear PA classes were compared, and the limitations of CMOS technology were discussed. Next, a linear Class A/AB CMOS PA model was designed in preparation for supply-tracking characterization in Chapter 3. Load-pull simulations were used to size the power device for power delivery. The P1dB and IMD performance of the final two-stage PA was optimized in order to effectively handle high PAPR modulation in WCDMA and LTE signals. A detailed modeling of the package and all passive elements was conducted while the PA is stabilized over a range of supply voltage and RF power at the desired load impedance.

Table 2.6: CW performance of CMOS PA at nominal 3.7V supply.

Technology	CMOS (device channel length = $0.34\mu m$
V_{DD} (V)	3.7
Frequency (MHz)	1950
Operating Class	A/AB
$P1dB$ (dBm)	27.4
$PAE_{@P1dB}$ (%)	36.4
$Gain$ (dB)	15.5
($IMD3$, $IMD5$)$_{@Pout}$(dBc)	(-29.2, -32.8) @ 21.6 dBm

Chapter 3

Modeling of Envelope and Average Power Tracking

3.1 Introduction

In Chapter 2, the design of the CMOS PA placed more emphasis on achieving high linearity rather than optimizing other performance metrics such as gain or efficiency. The main purpose was to prepare a working design model that would be able to handle complex modulated signals such as WCDMA and LTE. This chapter will commence with a description of key linearity characteristics of power amplifiers designed for non-constant envelope modulation. The impact of envelope and average power tracking on the performance of the CMOS PA in simulation is presented. Results from system-level simulations are provided.

3.1.1 Linearity Characteristics of Non-Constant Envelope Modulation

In Chapter 2, the linearity of the PA system is defined by its P1dB and IMD characteristics, assuming a simple continuous wave (CW) input or two-tone inputs. It is also important to understand how the PA can affect the quality of more complex signals (such as WCDMA or LTE modulation)

by observing and comparing the signal quality at both the input and output of the PA. Therefore, additional metrics of linearity will be introduced in this section, such as peak to average power ratio (PAPR), adjacent channel leakage-power ratio (ACLR) and error vector magnitude (EVM). The ACLR and EVM requirements are specified for both WCDMA and LTE digital communication standards (Chapter 1). The overall purpose of maintaining system linearity is to minimize signal distortion, thus enabling good connectivity and preventing corruption of neighboring channels.

3.1.1.1 PAPR

In high data rate standards, such as WCDMA and LTE that utilize a non-constant envelope signal, the instantaneous input power applied to the PA is varying in time. This variation in power is an inherent characteristic of the digital-modulated signal and places a major linearity constraint on the PA. A key metric used to quantify this variation is the peak-to-average power ratio (PAPR) which is defined as the ratio between the peak power and the average power of the signal for a given period of time. A statistical representation of the PAPR can be determined from a complementary cumulative distribution function (CCDF). It depicts the probability that the instantaneous power reaches a certain level. For example, 0.1% of the time, an input PAPR of 3.86dB is realized for WCDMA (Figure 3.1). The CCDF curves differ for each communication standard. A signal with larger PAPR requires more power back-off to maintain linear operation, to avoid compression of the PA.

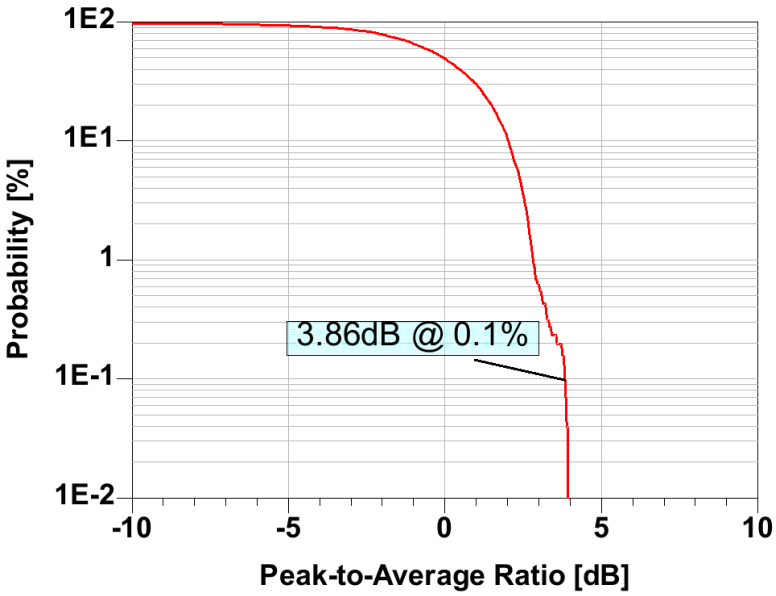

Figure 3.1: CCDF of WCDMA.

3.1.1.2 ACLR

Determining the output signal quality when the PA is driven with a non-constant envelope requires a detailed analysis. One of the most important metrics of linearity is the adjacent channel leakage-power ratio i.e., ACLR. It describes the amount of spectral regrowth that arises in neighboring channels due to odd-order intermodulation, which leads to a strong correlation between ACLR and IMD (Figure 3.2). This undesirable phenomenon interferes and potentially corrupts the signal quality of other users in the cell. The ACLR is calculated by taking the ratio of the integrated mean power in the main channel (centered at $F_{carrier}$) to the integrated mean power in the adjacent channel.

$$ACLR\,(dBc) = \frac{\int_{B_0} |P_{main\,channel}(f)|df}{\int_{B_1} |P_{adjacent\,channel}(f)|df} \tag{3.1}$$

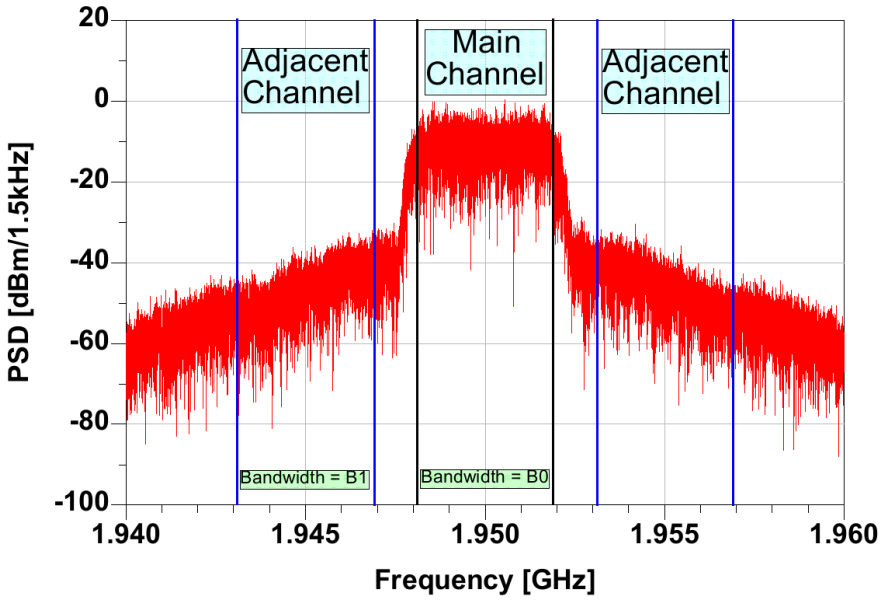

Figure 3.2: WCDMA spectrum displaying ACLR.

3.1.1.3 EVM

Another metric for linearity that describes the quality of the output signal is the error vector magnitude (EVM). This parameter illustrates the in-band distortion that arises in the PA and is strongly dependent on the digital modulation scheme. More specifically, it indicates how amplitude and phase distortions (AM-AM and AM-PM) in the PA increase the likelihood of incorrectly detecting the symbol constellation points which correspondingly degrades the system performance. EVM is defined as the distance between the

theoretical (ideal) I-Q symbol and the actual (measured) received I-Q symbol. Figure 3.3 displays the error vector magnitude and is typically represented as

$$EVM\,(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} * 100\% \tag{3.2}$$

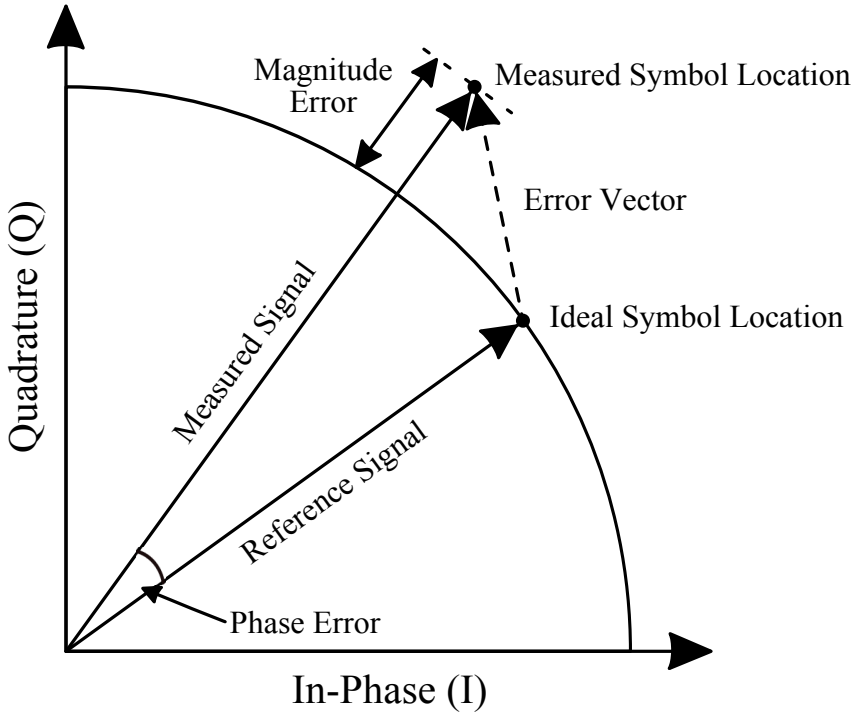

Figure 3.3: Error vector of I-Q symbols.

3.2 System-Level Simulations

System-level modeling allows engineers to efficiently evaluate and test concepts and algorithms while taking into consideration important system requirements and specifications. Creating a workflow that bridges system mod-

eling with actual design implementation can help to identify and correct for design flaws early in the design process, reduce verification time, and increase the rate of innovation.

In this study, the behavioral modeling of supply-tracking techniques for WCDMA and LTE are performed. The ADS Ptolemy tool is used for cosimulating behavioral DSP designs with analog/RF circuit designs.

3.3 ET and APT Simulation for 3GPP WCDMA

The baseband WCDMA I (in-phase) and Q (quadrature) components are created in the transmitter digital baseband, QAM modulated with a raised cosine filter and upsampled to form the RF continuous time-domain signal. As defined by the 3GPP Technical Specification *TS 25.101* document [18], the ACLR and EVM are simulated under the following conditions:

- *ACLR*: this measurement plots the main channel spectrum and the 5MHz/10MHz adjacent channels. The ACLR is calculated by taking the ratio of the main channel mean power (centered at $F_{carrier}$) to the adjacent channel mean power (centered at $F_{carrier}\pm$ 5MHz/10MHz). Each WCDMA channel spectrum is RRC filtered (excess bandwidth $\alpha = 0.22$) and integrated over a channel bandwidth of 3.84MHz. In compliance with [18], the $ACLR_{5MHz}$ and $ACLR_{10MHz}$ must be greater than 33dB and 43dB, respectively.

- *EVM*: this measurement calculates the error vector as the difference

between the theoretical input I-Q symbols and the actual output I-Q symbols. Both signals are passed through an RRC filter with a channel bandwidth of 3.84MHz and 0.22 roll-off factor. In compliance with [18], the EVM cannot exceed 17.5%. However, a much lower target is usually desired (4% in this study).

3.4 Average Power Tracking Behavioral Model

The system-level block diagram shown in Figure 3.4 consists of a behavioral model of *average power tracking* (APT). A numeric DSP constant voltage source is converted to the time domain through a *D/C* (discrete-to-continuous) converter and supplied to the PA, where both the driver and power stage are modulated.

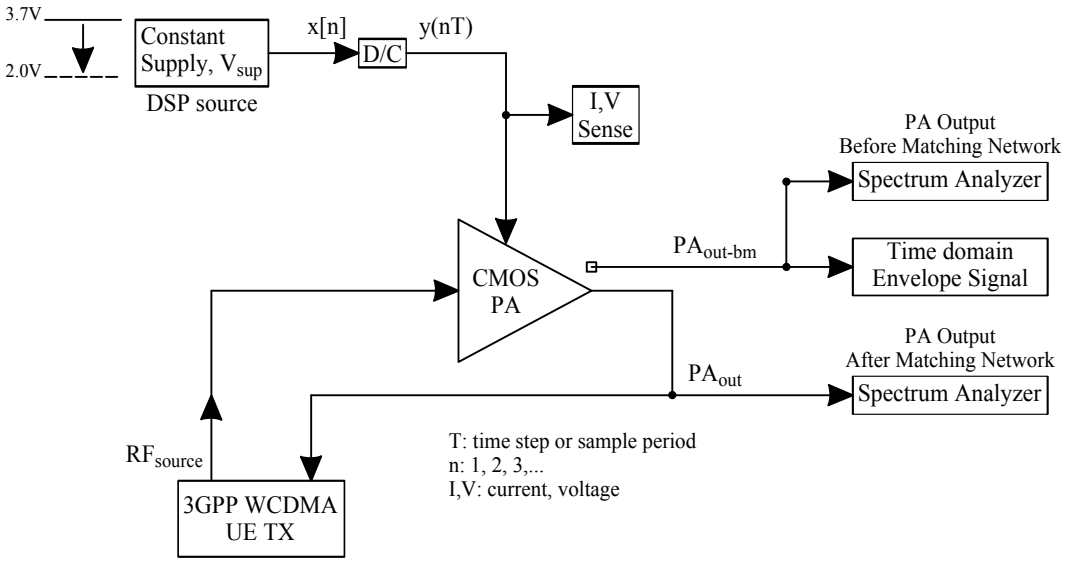

Figure 3.4: APT behavioral model.

As discussed in [28], this approach for efficiency enhancement is also referred to as *slow tracking*, and involves adjusting the fixed supply voltage near the largest peaks of the output envelope (Figure 3.5). Essentially, it tracks the change in PA average output power and is comparatively slower than envelope tracking. In this work, the APT supply modulator is implemented through a manual "measure/calibrate" algorithm.

- APT Algorithm

1. Initialize a set of input operating conditions:
   (a) V_{sup}: flat voltage supply rail (V)
   (b) RF_{source}: RF source power (dBm)
2. Measure the average output power (PA_{out}) and $ACLR$ after a simulation period of 1 time slot which is performed within the *3GPP WCDMA UE TX* module shown in Figure 3.4.
3. Manually modulate V_{sup} and tune RF_{source} to set the $ACLR_{5MHz}$ to -33dBc (WCDMA) for a given output power level.
4. Calculate power gain, DC power consumption and PAE.
5. Complete APT performance extraction over a wide range of output power levels (16dBm - 25dBm).

As will be discussed in Section 3.7, if there exists any ACLR headroom for the baseline 3.7V supply, the APT approach reduces the supply to the PA in order to recover any wasted efficiency. The PAE performance for an APT regime with ACLR calibration can then be compared to the battery connected (3.7V) PA.

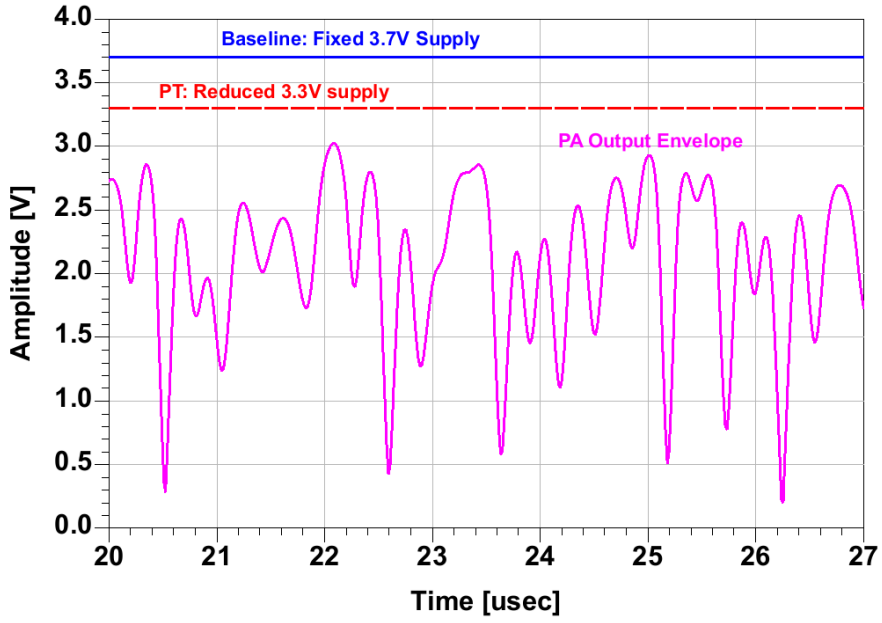

Figure 3.5: APT at Pout = 24dBm, WCDMA.

3.5 Envelope Tracking Behavioral Model

The second efficiency enhancement configuration that is investigated in this research is *envelope tracking* (ET) [28]. This involves supplying the PA with a voltage that instantaneously tracks the complex modulated envelope. The ET behavioral model for this scheme is shown in Figure 3.6.

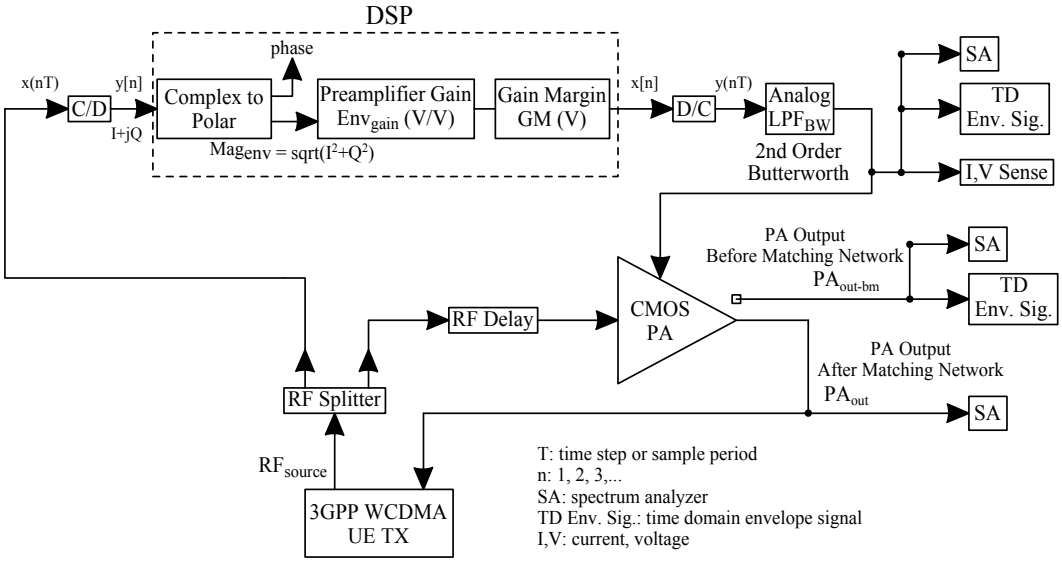

Figure 3.6: ET behavioral model.

The ET supply modulator is implemented mostly in the DSP with the exception of the LPF (low-pass filter). A lossless RF splitter couples the WCDMA RF signal to the envelope path in which a *C/D* (continuous-to-discrete converter) produces an equivalent WCDMA discrete signal to prepare for digital signal processing. Inside the DSP, the envelope is first detected through a *complex-to-polar* converter ($Mag_{env} = \sqrt{I^2 + Q^2}$). A preamplifier gain block compensates for the voltage gain through the PA. Its purpose is to behave as an ideal linear amplifier by amplifying the envelope supply signal to provide sufficient headroom above the PA output envelope signal. A gain margin block acts as a "fine-tuning" knob that allows tracking with more margin. It is noted that the PA supply envelope is to be compared with the PA output envelope at the drain before the matching network, and not the

final amplified voltage envelope at the 50Ω termination. To compensate for the delay in the envelope path, a delay element is placed in the RF input path. The envelope signal is converted back into the continuous-time domain. A 2nd order Butterworth LPF allows for adjustment in the bandwidth of the supply envelope.

The non-linear operation which extracts the magnitude of the envelope from the RF input I/Q signal results in an expansion of bandwidth in the supply envelope path. A bandwidth of approximately 2MHz is observed for half of the upconverted RF WCDMA I/Q spectrum (Figure 3.7). The bandwidth of the supply envelope is then expanded by 3.4 times as shown in Figure 3.8. Due to the bandwidth expansion, the supply modulator can become a design bottleneck for wide bandwidth applications [29]. However, unlike in EER, the design of the modulator can potentially be relaxed in ET since the envelope signal does not have to be replicated with great accuracy. Hence, the impact that reduced tracking bandwidth has on the performance of the PA can be studied.

Figure 3.9 shows the power spectral density (PSD) of a single-carrier WCDMA supply envelope signal before and after the introduction of an LPF with a passband frequency of 5MHz and stopband frequency of 6MHz. The majority of the energy in the original envelope is located near DC. The LPF retains most of the energy which is located at low frequencies, and filters out the energy at higher frequencies.

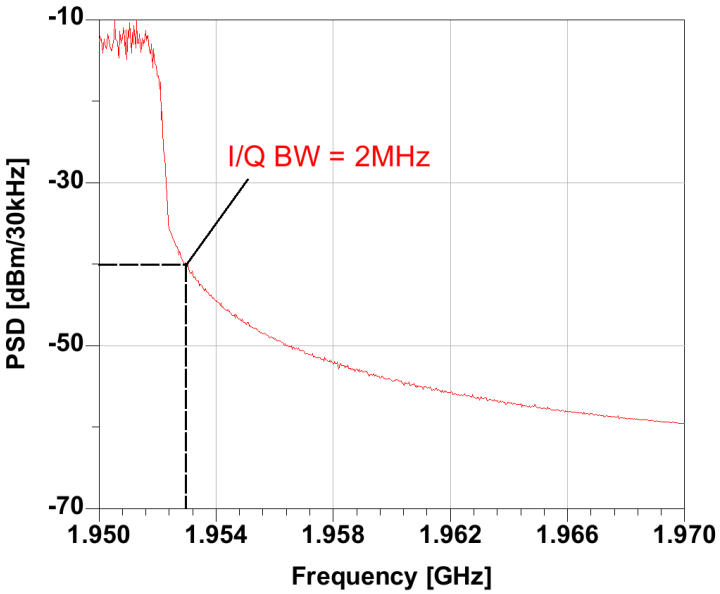

Figure 3.7: RF input I/Q WCDMA spectrum.

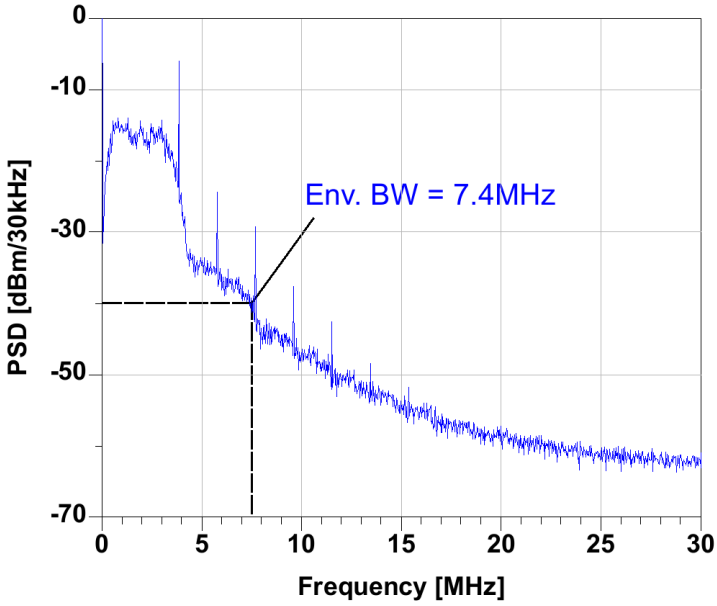

Figure 3.8: Supply envelope WCDMA spectrum with expanded bandwidth (full scale of the DC component is not shown).

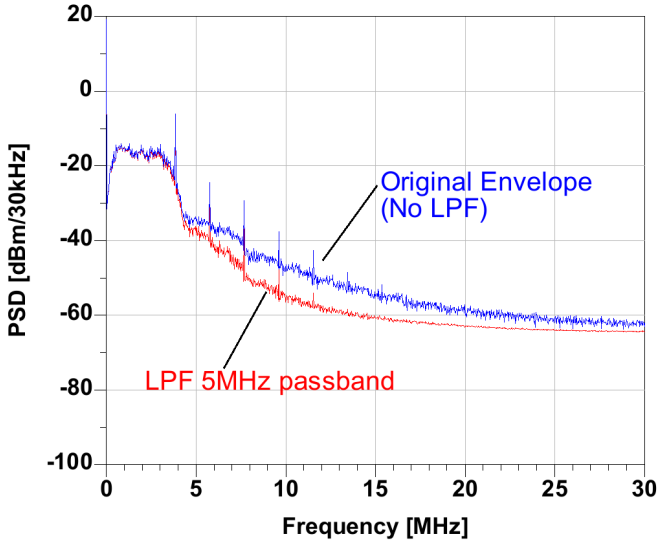

Figure 3.9: Supply envelope WCDMA spectrum with/without LPF 5MHz passband frequency.

More insight can be provided by examining the behavior of reduced bandwidth supply envelopes in the time-domain. The following three cases are considered:

- no LPF
- with LPF 5MHz passband
- with LPF 3MHz passband

The first observation is the offset between the envelopes (Figure 3.10), which is due to an increase in group delay as the passband frequency of the LPF decreases. This means that the RF input delay must be adjusted correspondingly to prevent a misalignment in the RF and supply envelopes and

degradation in ACLR. Second, a smaller LPF bandwidth limits the tracking precision including how deep the supply envelope tracks the troughs and how high it tracks the peaks of the signal. Even though a 3MHz supply envelope may be a simpler signal to implement in hardware, a reduction in tracking bandwidth does not occur without a sacrifice in PA linearity. Table 3.1 summarizes the $ACLR_{5MHz}$ performance for a WCDMA input signal at an output power of 24dBm. The ACLR is degraded as the LPF cutoff frequency is reduced down to 3MHz. Gaining a better understanding of this trend can help define the tracking bandwidth requirement in the supply modulator. For this study, the LPF passband frequency will be set to 5MHz and 10MHz for WCDMA and LTE 10MHz, respectively, and the RF and supply envelopes will be properly aligned.

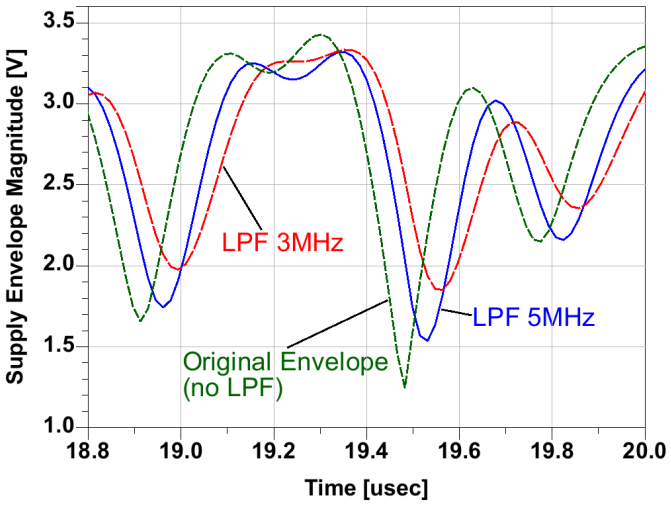

Figure 3.10: WDCMA supply envelope magnitude for various LPF passband frequencies.

Table 3.1: WCDMA PA linearity with reduced supply envelope bandwidth.

Configuration	no LPF	with LPF 5MHz	with LPF 3MHz
Pout (dBm)	24.2	24.1	24.1
$ACLR_{-5MHz}$ (dBc)	-34	-33.5	-31.3
$ACLR_{+5MHz}$ (dBc)	-34.1	-33.7	-32.4

An example of the envelope tracking behavior is illustrated in Figure 3.11. For this specific example, the passband frequency of the LPF is fixed at 5MHz to pass through the entire WCDMA spectrum. The group delay of the filter is then compensated with an RF delay in order to minimize timing mismatch between the RF and supply paths.

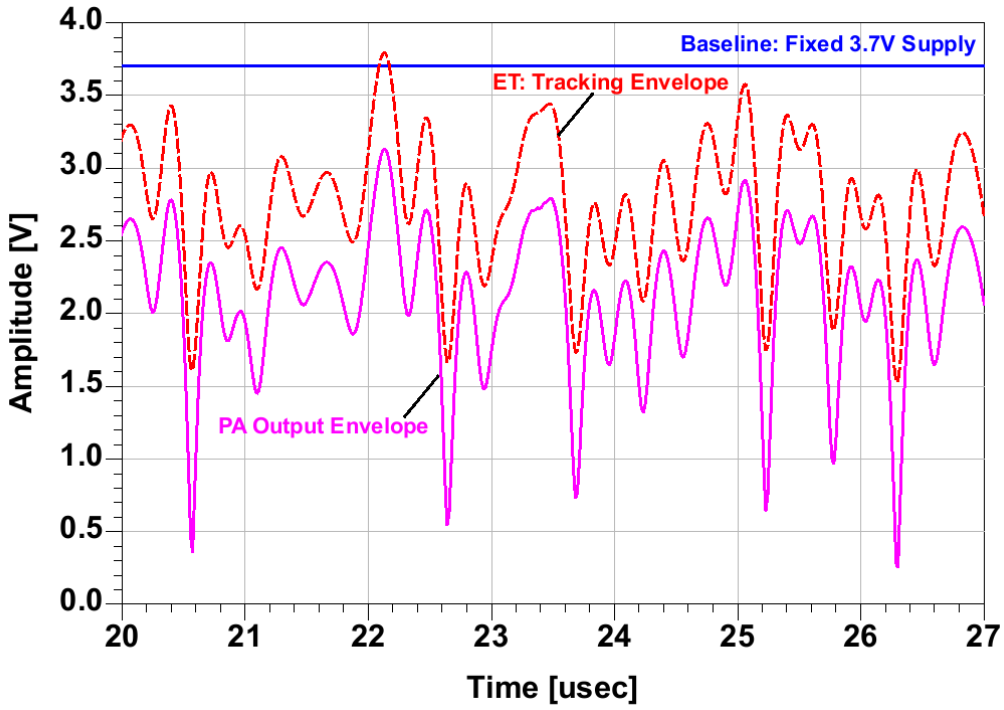

Figure 3.11: Fixed supply vs. ET at Pout = 24dBm, WCDMA.

Similar to the APT model, a manual "measure/calibrate" algorithm is used for ET. However, it should be noted that unlike average power tracking, the $ACLR_{5MHz}$ is not calibrated to a specific value since ET essentially linearizes the PA over a range of power levels. Instead, the power gain is calibrated over a wide range of output power. Since there are several degrees of freedom when adjusting these supply modulator parameters, many different ET methodologies can be implemented. The precise approach taken in this work is shown below.

- ET Algorithm

1. Initialize a set of input operating conditions:
   (a) RF_{source}: RF source power (dBm)
   (b) Env_{gain}: preamplifier gain (V/V)
   (c) GM: gain margin (V)
   (d) LPF_{BW}: low-pass filter bandwidth (MHz)
2. The Env_{gain} is properly fixed to a magnitude that ensures linear operation of the PA over a range of power levels.
3. The LPF_{BW} is set to the tracking bandwidth that is desired.
4. While RF_{source} is incremented by 1dB to sweep output power levels, the GM can be slightly tuned to calibrate the power gain of the PA.

5. Measure the average output power (PA_{out}) and $ACLR$ after a simulation period of 1 time slot.

6. Calculate power gain, DC power consumption and PAE.

7. Complete ET performance extraction over a wide range of output power levels (16dBm - 26dBm).

3.6 ET and APT Simulation for 3GPP LTE

Since power consumption is more of a concern for LTE user equipment terminals, the uplink transmission is based on a SC-FDMA scheme with reduced PAPR and an FDD frame structure. The three modulation types that are supported are: QPSK, 16QAM and 64QAM. Also a variety of channel bandwidths are offered: 1.4MHz, 3MHz, 5MHz, 10MHz, 15MHz and 20MHz. Similar to WCDMA, the discrete baseband I-Q LTE signals are QAM modulated (without a RC filter) to form the RF continuous time-domain signal.

Some key distinctions in the measurement of the linearity performance for LTE are explained in this section. As defined by the *ETSI TS 136 101* technical specification [20] document, the ACLR for LTE is measured as follows:

- *ACLR*:

  - E-UTRA vs. E-UTRA: This measurement plots the $E-UTRA_{main}$ (LTE main) channel spectrum and the $E-UTRA_{L1/H1}$ (LTE ad-

jacent) channels. The ACLR is calculated by taking the ratio of the main channel mean power (centered at $F_{carrier}$) to the adjacent channel mean power (centered at $F_{carrier} \pm$ channel BW). Each LTE channel spectrum is placed through a rectangular filter and is integrated over a measurement bandwidth that varies with channel bandwidth. In compliance with [20], the $E-UTRA\,ACLR_{L1/H1}$ must be greater than 30dBc.

– E-UTRA vs. UTRA: This measurement plots the $E-UTRA_{main}$ (LTE main) channel spectrum and the $UTRA_{L1/H1}$ and $UTRA_{L2/H2}$ (WCDMA adjacent) channels. The ACLR is calculated by taking the ratio of the main channel mean power (centered at $F_{carrier}$) to the adjacent channel mean power (centered at $F_{carrier} \pm$ channel BW). The $E-UTRA_{main}$ spectrum is placed through a rectangular filter and is integrated over a measurement bandwidth that varies with channel bandwidth. The $UTRA_{1,2}$ spectrum is RRC filtered (excess bandwidth $\alpha = 0.22$) and integrated over a channel bandwidth of 3.84MHz. In compliance with [20], the $UTRA\,ACLR_{L1/H1}$ and $UTRA\,ACLR_{L2/H2}$ must be greater than 33dBc and 36dBc, respectively.

3.7 Simulation Results

In this section, a variety of simulation results are presented through an extensive characterization of the CMOS PA. First, the PA performance

is analyzed with a WCDMA 3.84MHz signal. The efficiency and linearity performance is compared for the three regimes: fixed 3.7V, average power tracking, and envelope tracking. Next, the PA is characterized with an LTE 10MHz 64QAM signal and the results are compared to those from WCDMA. Finally, some key observations based on this investigation are discussed.

3.7.1 WCDMA

The following results are based off of the APT and ET algorithms that are proposed in Sections 3.4 and 3.5. As shown in Figure 3.12, the power gain is calibrated near 15.3dB (backed-off from 1dB compression point) for the ET regime, while the standalone and APT approaches have similar gain characteristics as was observed for a CW input. The gain expansion is more accentuated at lower supply voltage while performing APT.

The results in Figure 3.13 display the potential maximum improvement in PAE over output power for an ideal supply modulator (100% efficiency). ET achieves a peak improvement of 15% from 21-22 dBm, while APT improves the PAE by a maximum of 9.8% at 19dBm. In comparison to the fixed-supply case, average power tracking is more beneficial at lower output power levels while envelope tracking is more beneficial at higher power levels. At 21dBm, the supply modulator needs to be at least 40% efficient for ET to show any efficiency improvement. However at 25dBm, the modulator must be more than 81.5% efficient for ET to provide a competitive solution.

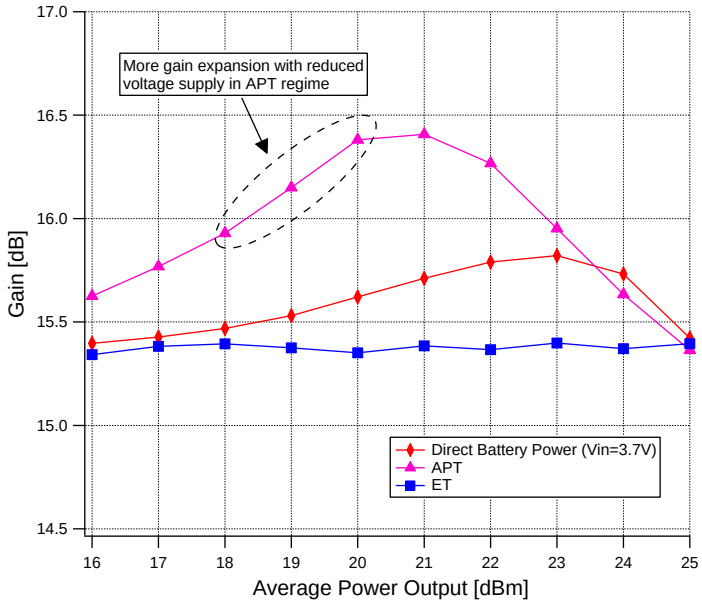

Figure 3.12: Power gain for different regimes, WCDMA input.

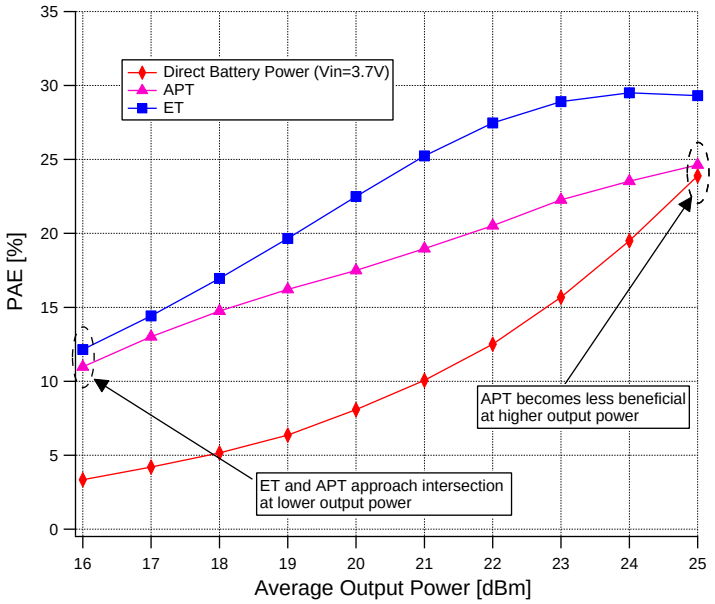

Figure 3.13: WCDMA PAE comparison: ET, APT vs. fixed 3.7V supply.

Figure 3.14 displays the $ACLR_{5MHz}$ behavior of the PA in APT mode compared to the baseline fixed-supply operation. The ACLR response for the stand-alone PA is very similar to the IMD behavior seen in Chapter 2. The WCDMA signal begins to compress the PA at 23dBm as the ACLR degrades more rapidly. In the APT regime, all the ACLR headroom is exchanged for additional efficiency, and the maximum amount of PAE is recovered by setting the $ACLR_{5MHz}$ to -33dBc.

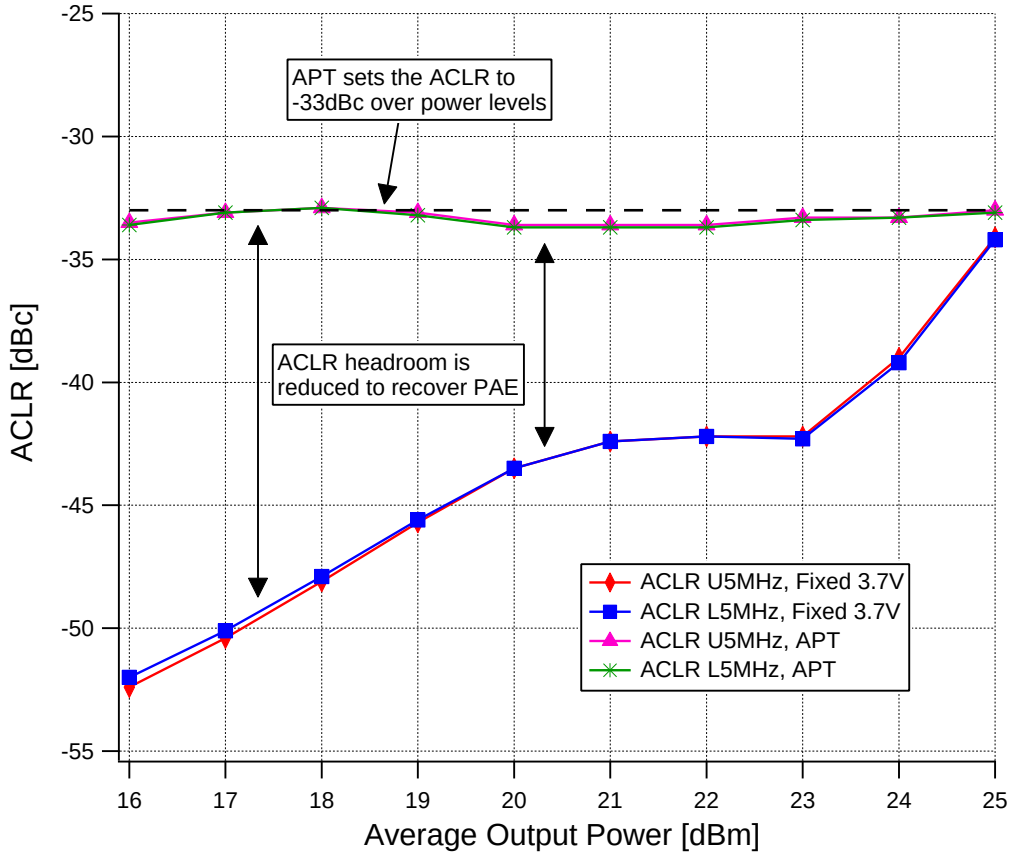

Figure 3.14: WCDMA $ACLR_{5MHz}$ comparison: APT vs. fixed 3.7V supply.

Even though the gain of the PA is fixed over output power in envelope tracking mode (Figure 3.12), the ACLR degrades at high output power levels (Figure 3.15). In the back-off region, not only is ET more power efficient than APT, but it also maintains an ACLR cushion. However, the PA is more easily compressed with a WCDMA envelope than a CW signal and approaches the -33dBc limit at higher output power levels. As shown in Figure 3.16, the EVM is below 4% over output power and follows similar trends as the ACLR for both APT and ET regimes.

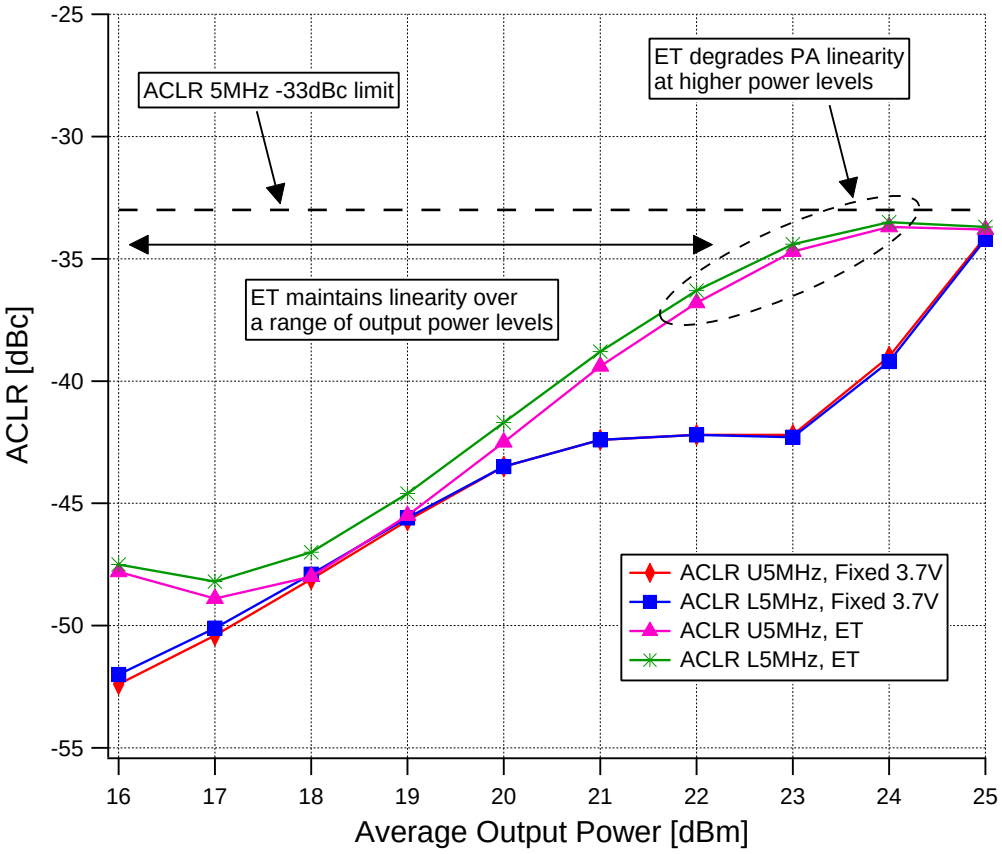

Figure 3.15: WCDMA $ACLR_{5MHz}$ comparison: ET vs. fixed 3.7V supply.

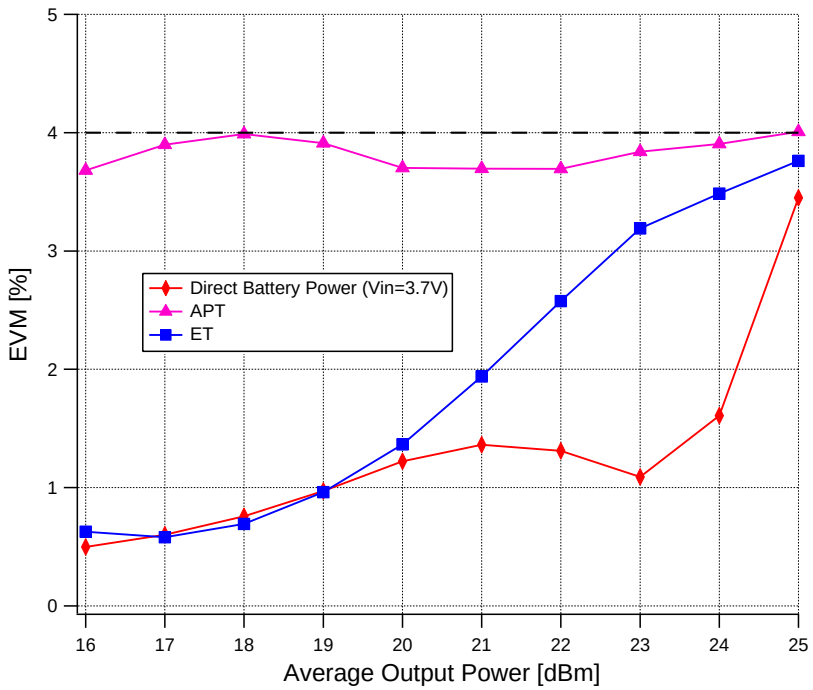

Figure 3.16: WCDMA EVM comparison: ET, APT vs. fixed 3.7V supply.

3.7.2 LTE

The same APT and ET algorithms are used for LTE. A slight adjustment is made in the ACLR calibration for the APT algorithm ($E-UTRA\,ACLR_{L1/H1}$ is set near -30dBc). CMOS PA performance for an LTE signal is analyzed in this section. Table 3.2 shows a large increase in the PAPR from WCDMA to LTE. Additionally, the PAPR is seen to vary with modulation scheme. In LTE, the highest data rate is achieved with 64QAM modulation and yields the largest PAPR of 6.55dB (0.1% peak power level). This is considered the worst case scenario, in which the linearity of PA is affected the most.

Table 3.2: PAPR comparison of WCDMA and LTE.

Signal	**PAPR (dB)**
WCDMA 3.84MHz	3.86
LTE 10MHz QPSK	5.76
LTE 10MHz 64QAM	6.55

The PAE results for the LTE driven PA are shown in Figure 3.17. The intersection where APT is as efficient as the fixed 3.7V supply regime occurs at an average output power of approximately 24dBm. Beyond this point, there is no incentive in applying APT. Furthermore, Figure 3.18 indicates that APT is less effective over all power levels for LTE. However, envelope tracking shows similar PAE improvements for both WCDMA and LTE.

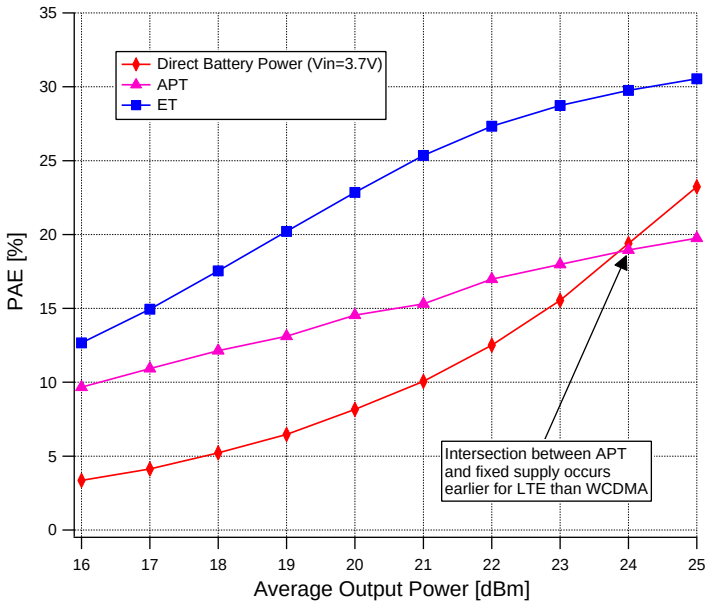

Figure 3.17: PAE comparison: ET, APT vs. fixed 3.7V supply, LTE 10MHz 64QAM input.

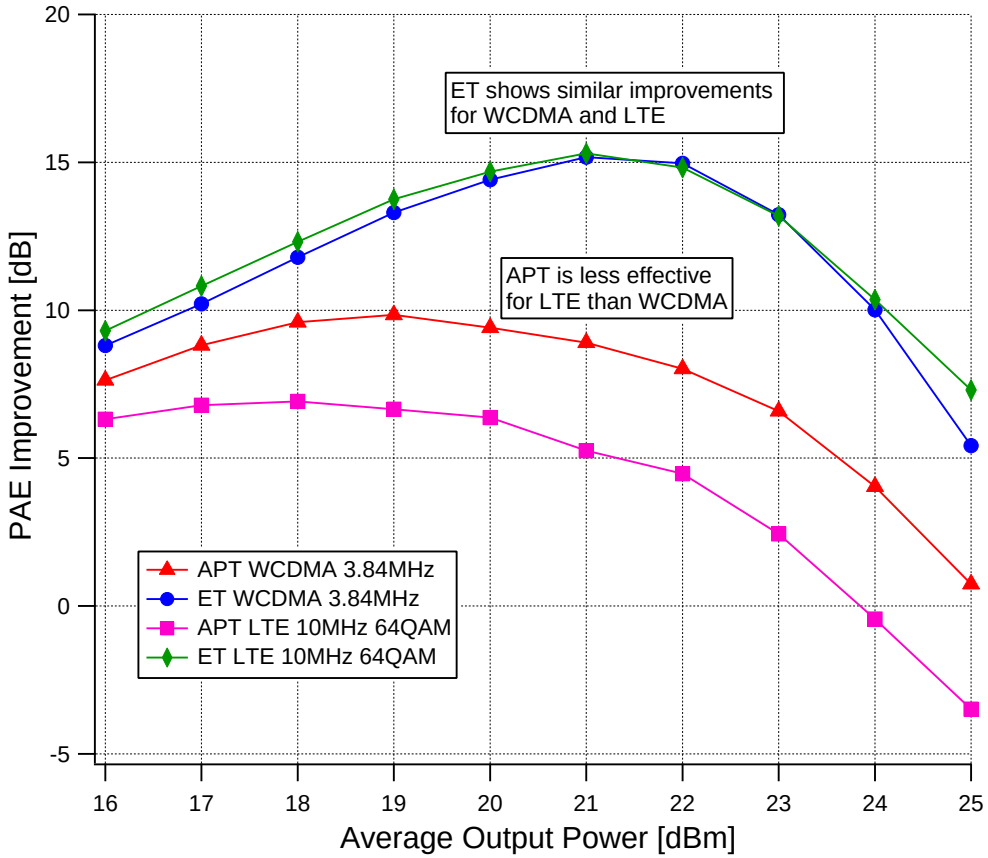

Figure 3.18: PAE improvement: ET, APT vs. fixed 3.7V supply, WCDMA 3.84MHz vs. LTE 10MHz 64QAM.

Figure 3.19 describes how the larger PAPR signal impacts the PA's linearity. The most stringent linearity specification for LTE is $E-UTRA\,ACLR_1$ (LTE main channel vs. LTE adjacent channel). The results for $UTRA\,ACLR$ are not displayed since they easily pass the requirement over all power levels. In comparison to WCDMA, the fixed-supply PA for LTE has much less ACLR headroom in the back-off region, and it begins to fail the -30dBc requirement at 24dBm. In addition, average power tracking can only be fixed to -30dBc

up until 24dBm. Beyond that output power level, the power amplifier is not linear enough for APT mode since the larger PAPR signal causes the PA to compress more.

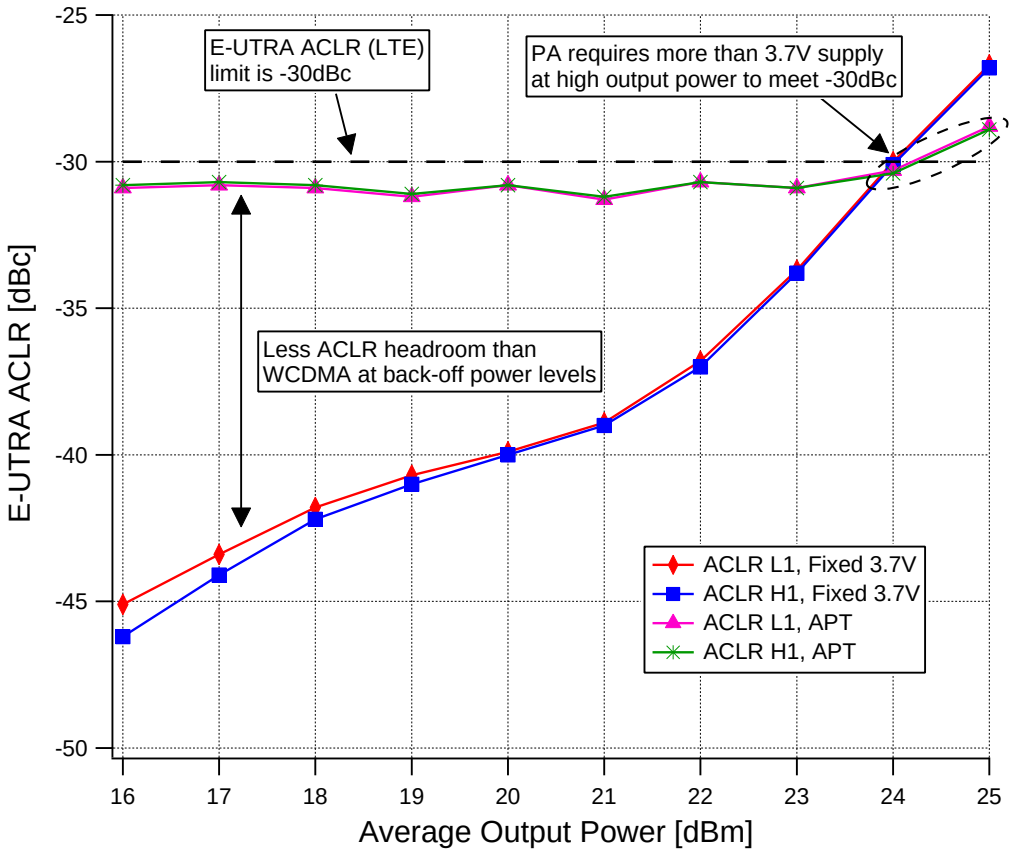

Figure 3.19: $E-UTRA\,ACLR_1$ comparison: APT vs. fixed 3.7V supply, LTE 10MHz 64QAM input.

Similarly, the PA in ET mode also suffers from additional nonlinearity in LTE applications. It begins failing the $E-UTRA\,ACLR_1$ specification as early as 22.5dBm. The high-frequency rising and falling edges of the LTE envelope are more difficult to track with symmetry due to the low-pass filtering

of the envelope and timing misalignment that may exist between the RF and envelope paths. This results in asymmetrical energy in the low and high adjacent LTE channels as shown in Figure 3.20.

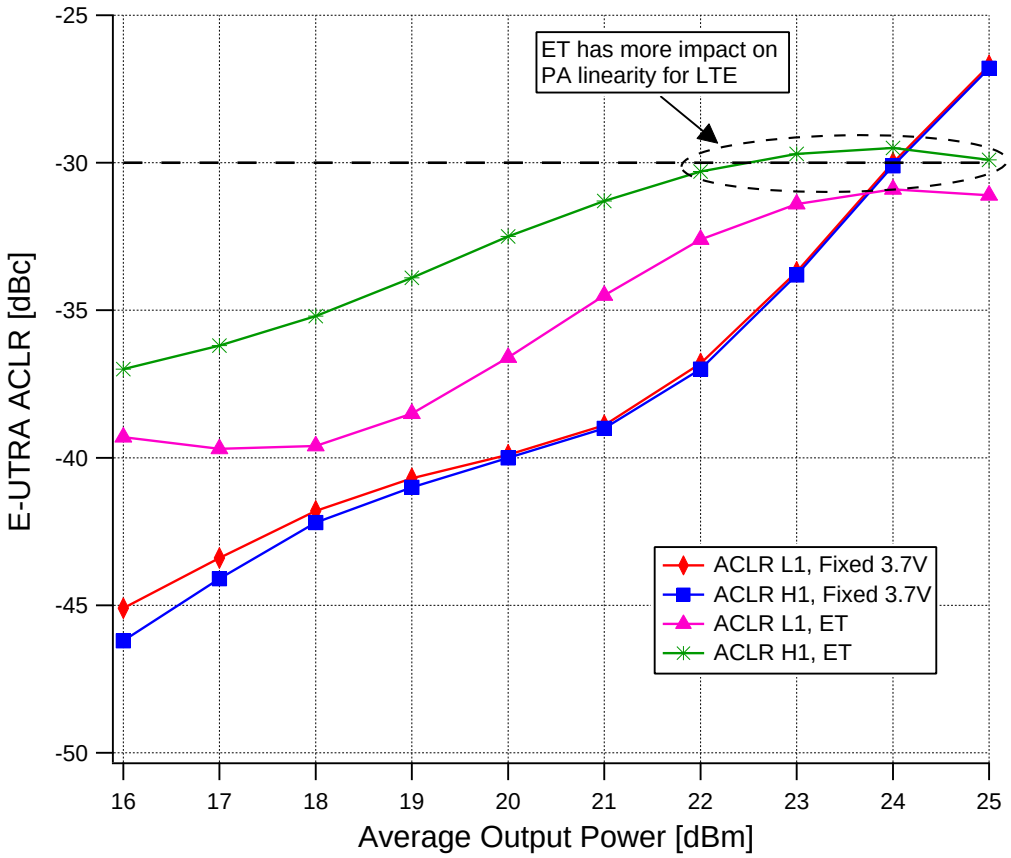

Figure 3.20: $E-UTRA\,ACLR_1$ comparison: ET vs. fixed 3.7V supply, LTE 10MHz 64QAM input.

3.8 Conclusion

In this chapter, key linearity characteristics of non-constant envelope modulation, (PAPR, ACLR, and EVM) were introduced. The focus of this

portion of the thesis was on a system-level analysis of various supply-tracking techniques on the CMOS PA that was designed in Chapter 2. Algorithms are developed for both envelope and average power tracking and implemented through behavioral models. Each supply-tracking regime is analyzed for both WCDMA and LTE, and the efficiency and linearity performance of the PA are compared in simulation. The important observations of this investigation are divided into WCDMA and LTE and summarized as follows:

WCDMA

- Converting the WCDMA I/Q envelope signal to a supply envelope signal results in a bandwidth expansion of 3.4 times. The passband frequency of a low-pass filter placed in the supply path is varied to better understand the impact that a reduction in bandwidth has on the linearity of the PA. The conclusion is that ACLR degrades with reduced bandwidth.

- A peak PAE improvement of 15% is observed at output power levels of 21-22 dBm when transitioning from a fixed 3.7V supply to an ET mode. In comparison, APT provides a maximum improvement of 9.8% at 19dBm. These improvements are based off the assumption that the supply modulator is 100% efficient. In practice, the supply modulator efficiency will impact the overall system efficiency gains.

- Average power tracking is less beneficial at higher output power levels, while the benefit of ET at lower power levels is similar to APT.

- APT exchanges any ACLR headroom for additional efficiency by fixing the $ACLR_{5MHz}$ to the limit of -33dBc. In ET mode, the ACLR is improved in back-off power regions, however, as the PA approaches compression, the $ACLR_{5MHz}$ approaches the specification limit.

- The EVM is below 4% over output power for WCDMA, and its behavior follows the same trends as the ACLR for both envelope and average power tracking.

LTE

- The PAE improvements for the ET PA are very similar for LTE and WCDMA, yet the PA linearity is degraded more for LTE. This is apparent in the $E-UTRA\,ACLR_1$ plot which begins failing at 22.5dBm.

- APT is more effective for WCDMA than LTE over all power levels.

Chapter 4

Conclusion

The two most important characteristics of power amplifiers for wireless handset applications are efficiency and linearity. Several efficiency enhancement approaches have been proposed and implemented over the years to help address critical handset issues such as reduced battery life and excessive thermal dissipation. In this thesis, the primary focus is to investigate the concepts of envelope and average power tracking in order to improve the efficiency of a CMOS power amplifier while ensuring an acceptable level of linearity degradation. This simulation-based study is conducted for two of the most popular communication standards used in today's cellular industry, WCDMA and LTE. The important achievements of this thesis can be summarized as follows:

- A linear Class A/AB power amplifier is designed in a CMOS process. This class of operation is a promising candidate for supply-tracking operation especially in high PAPR applications such as WCDMA and LTE. A load-pull design methodology is used to study the power delivery capabilities of the power device. A practical TQFN package is included in the design of the full PA. All non-integrated passive elements employ practical commercial models. The package and lumped-element para-

sitics are seen to reduce the overall gain and efficiency of the PA. When operating at $V_{DD} = 3.7$V, the power amplifier is capable of delivering an output power of 27.4dBm with 36.4% PAE in simulation. The third and fifth-order intermodulation distortion is -29dBc and -33dBc at a back-off power level of 21.6dBm.

- A system-level analysis incorporating the co-simulation of digital communication standards and the power amplifier is enabled with the use of ADS Ptolemy. The behavioral models of envelope and average power tracking are implemented based on the developed algorithms. Each supply-tracking regime has a considerable impact on the performance of the PA. Furthermore, the high PAPR characteristic of non-constant WCDMA and LTE envelope signals degrades the linearity especially at higher output power levels. Some of the key observations that can be drawn from this study are as follows:

- In comparison to the fixed 3.7V supply PA, a peak PAE improvement of 15% at output power levels between 21-22 dBm is achieved when applying envelope tracking for WCDMA. Average power tracking renders an efficiency gain of 9.8% at 19dBm, however it is seen to offer no advantage at higher output power. Envelope tracking becomes less beneficial at lower output power as it approaches similar PAE as average power tracking. These results are presented with the assumption that an ideal 100% efficient supply modulator is realized. However in practice, any

efficiency loss in the modulator will reduce the overall efficiency gains provided by ET or APT. Regarding linearity, in APT mode, the PA operates on the $ACLR_{5MHz}$ limit of -33dBc. On the other hand, ET provides $ACLR_{5MHz}$ headroom in back-off power and approaches the specification limit as it is pushed towards compression. The EVM is below 4% over output power for both envelope and average power tracking.

- The trends observed for WCDMA 3.84MHz are compared to LTE 10MHz 64QAM application. Envelope tracking achieves similar PAE enhancement for LTE, however the PA linearity is degraded more for a larger PAPR in LTE. This is visible as the $E-UTRA\,ACLR_1$ begins failing the -30dBc specification at 22.5dBm. The average power tracking trends over output power are similar for both standards, yet APT provides less overall PAE improvement for LTE than WCDMA.

CMOS PAs have already narrowed the gap to III-V technologies in the area of 3G. However, transitioning to 4G translates into the requirement for higher linearity which becomes challenging in the CMOS realm. New design architectures are required to enable very linear CMOS PAs that can be combined with high efficiency ET supply modulators to improve the battery life of LTE handsets. Introducing digital predistortion can further aid in maintaining good linearity while effectively performing these supply-tracking techniques.

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